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Increasing MMIC Yield with Advanced Statistical Design Methods

November 8, 2001

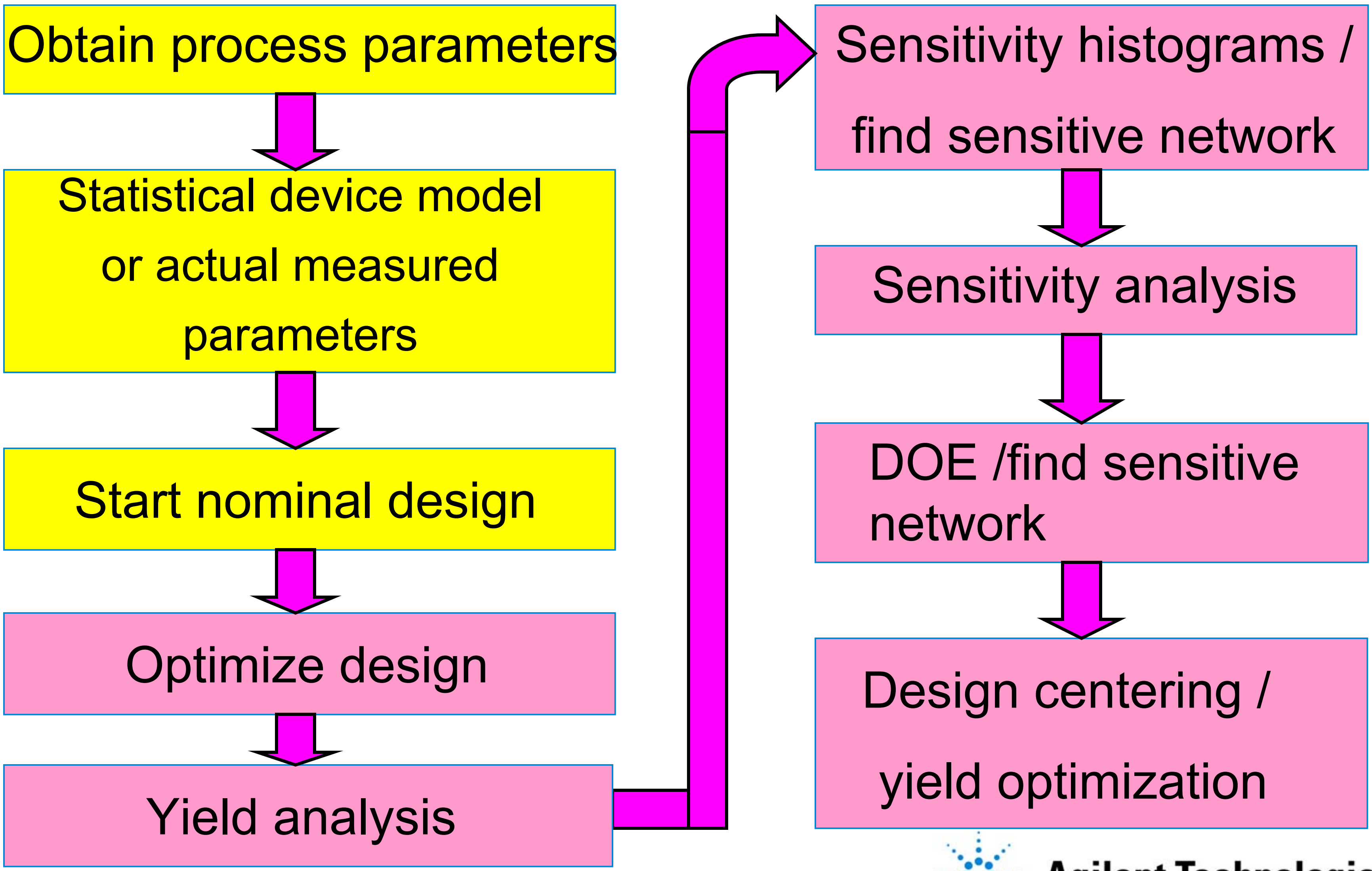
presented by:

Jack Sifri

Agenda

- **Initial Design Process of X-band LNA**
  - ***X-band LNA Elements***
  - ***Programmable Optimization***
  - ***Yield Analysis***
- **Statistical Tools for Robustness**
  - ***Yield Sensitivity Histograms***
  - ***Sensitivity Analysis***
  - ***Design of Experiments***
  - ***Yield Optimization (Design Centering)***
- **Final LNA Design**

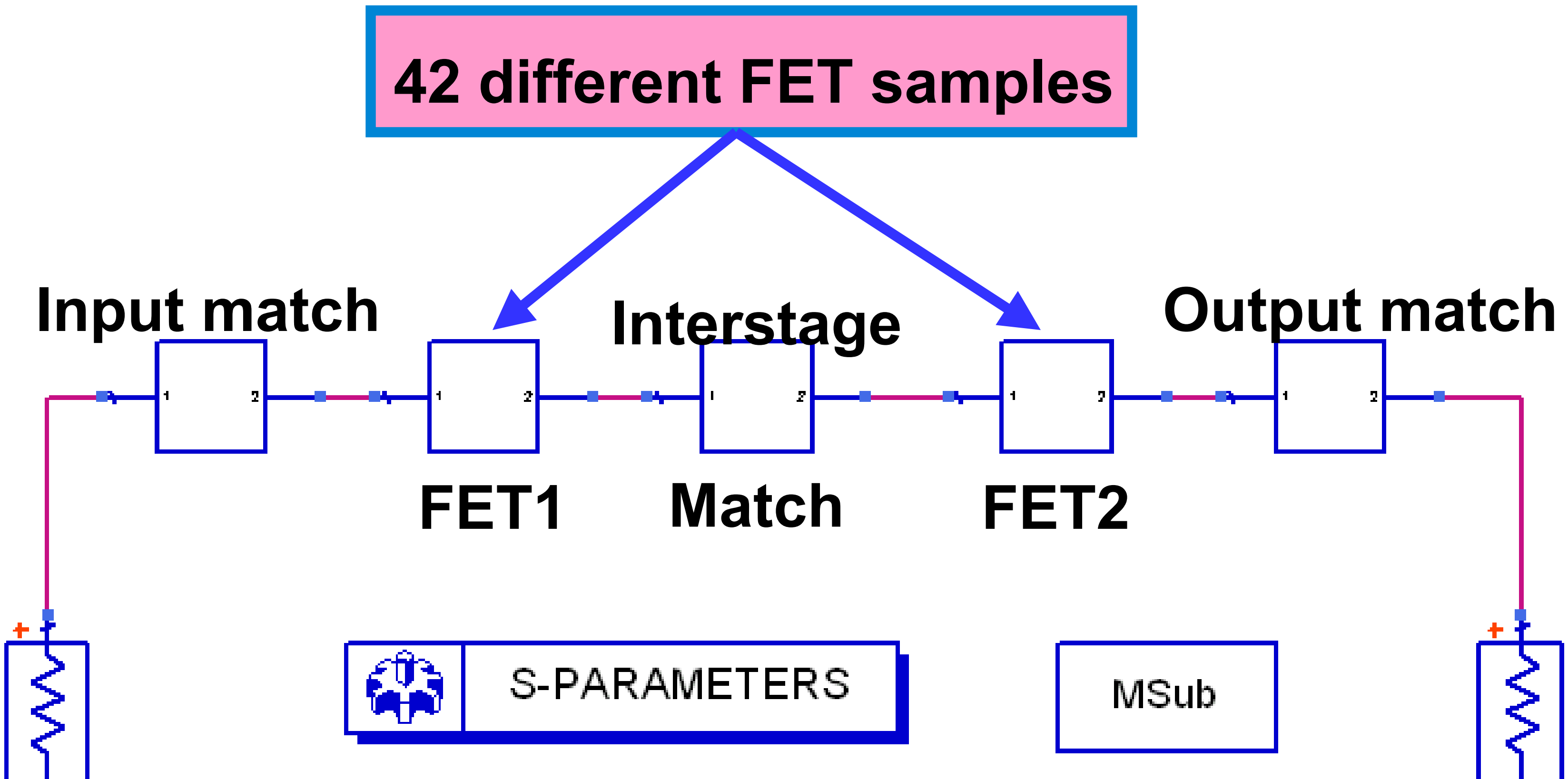
MMIC Statistical Design Process



X-Band LNA Specifications

• Center frequency (Fc)	8 GHz
• Bandwidth (20%)	7.2 - 8.8 GHz
• Gain (S21)	> 14 dB
• Noise figure (NF)	< 3 dB
• Output return loss (S22)	< -14 dB

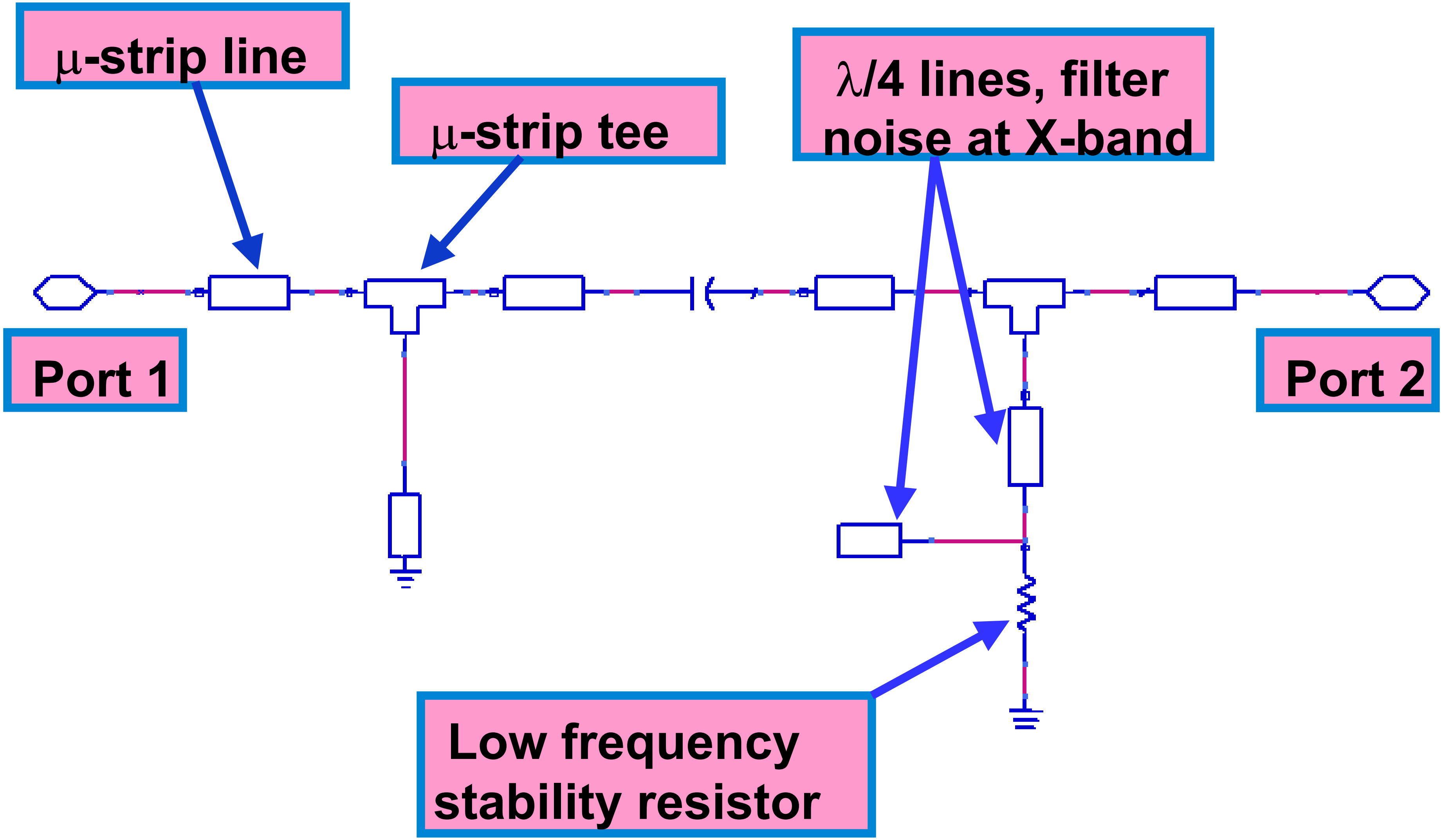
X-Band LNA Top-Level Schematic



- 5% Gaussian variation in lumped
- Line widths vary ± 1/2 um
- Substrate height 100 um ± 3 um
- Substrate Er 12.9 ± 5%
- 42 FET samples

Process parameters

Input Matching Network for Noise



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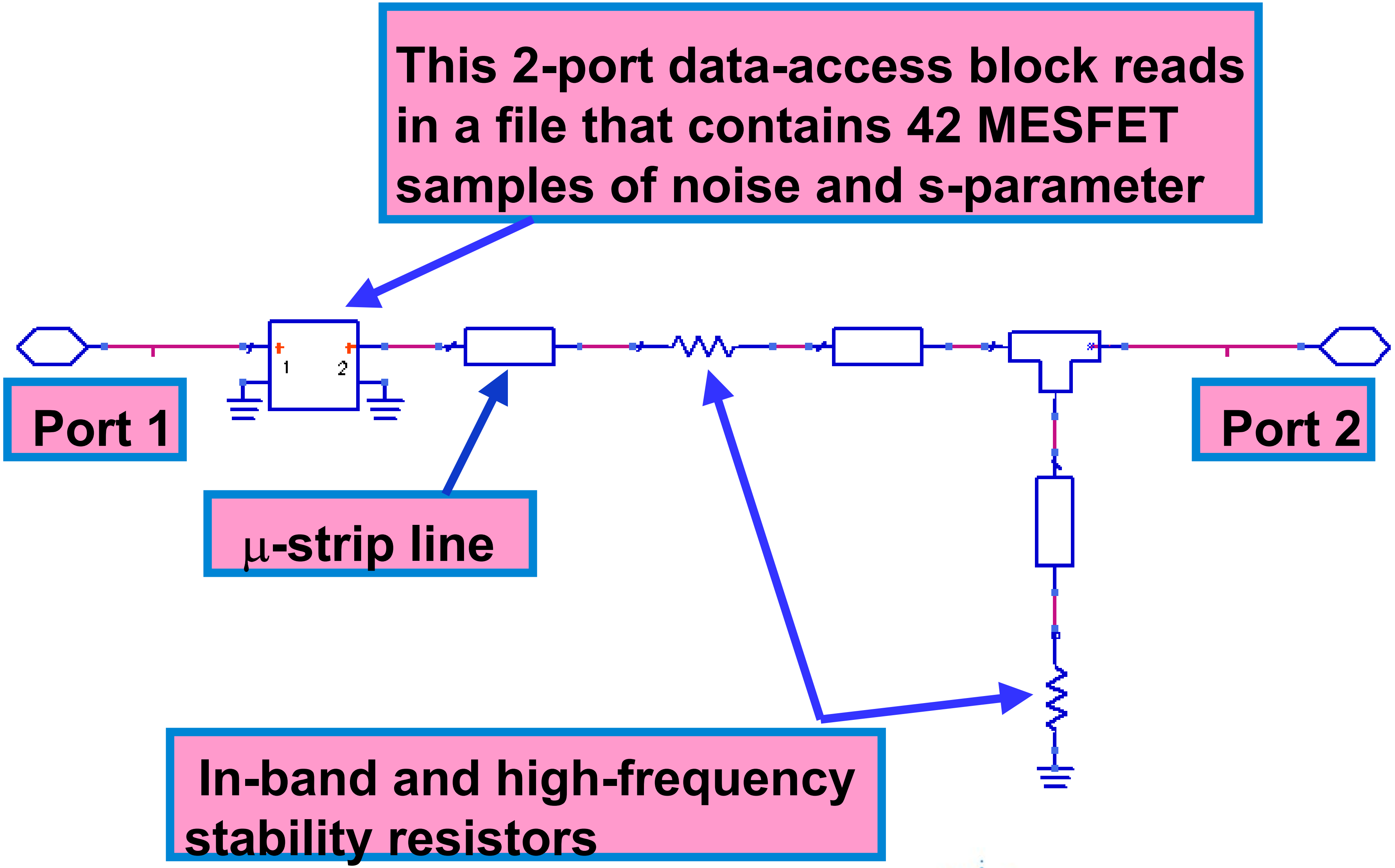
FET1 Structure with Stability Resistors



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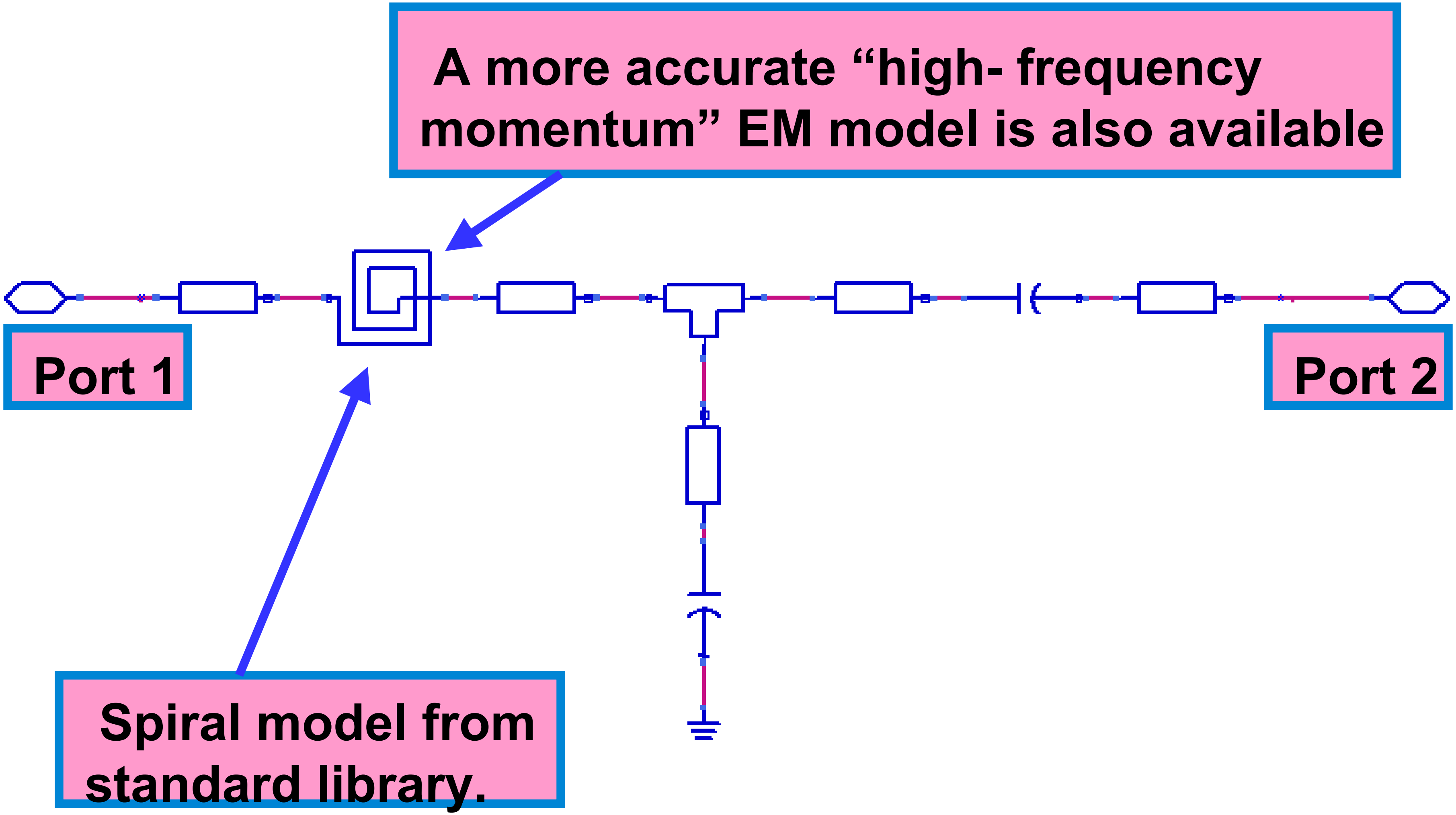
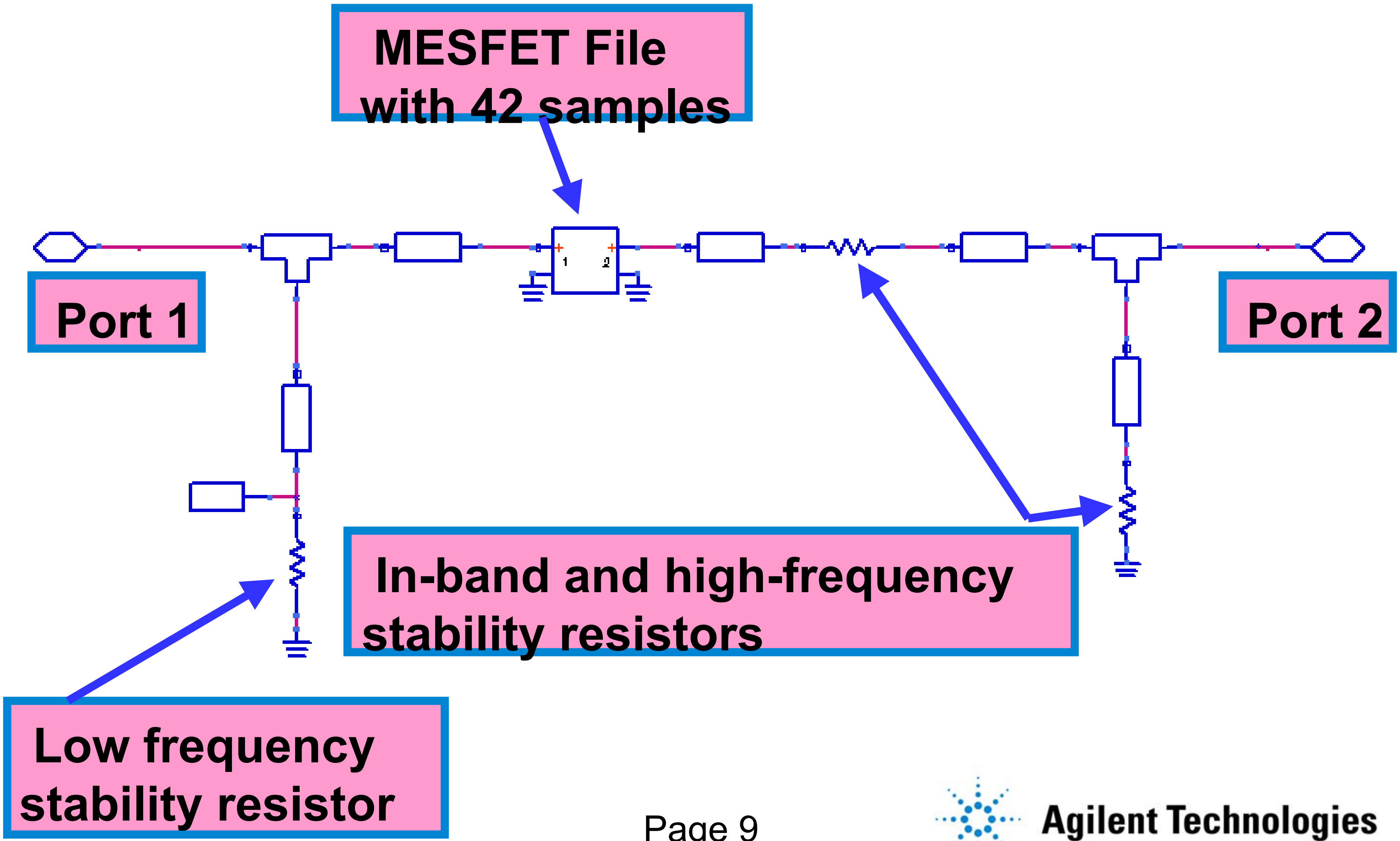
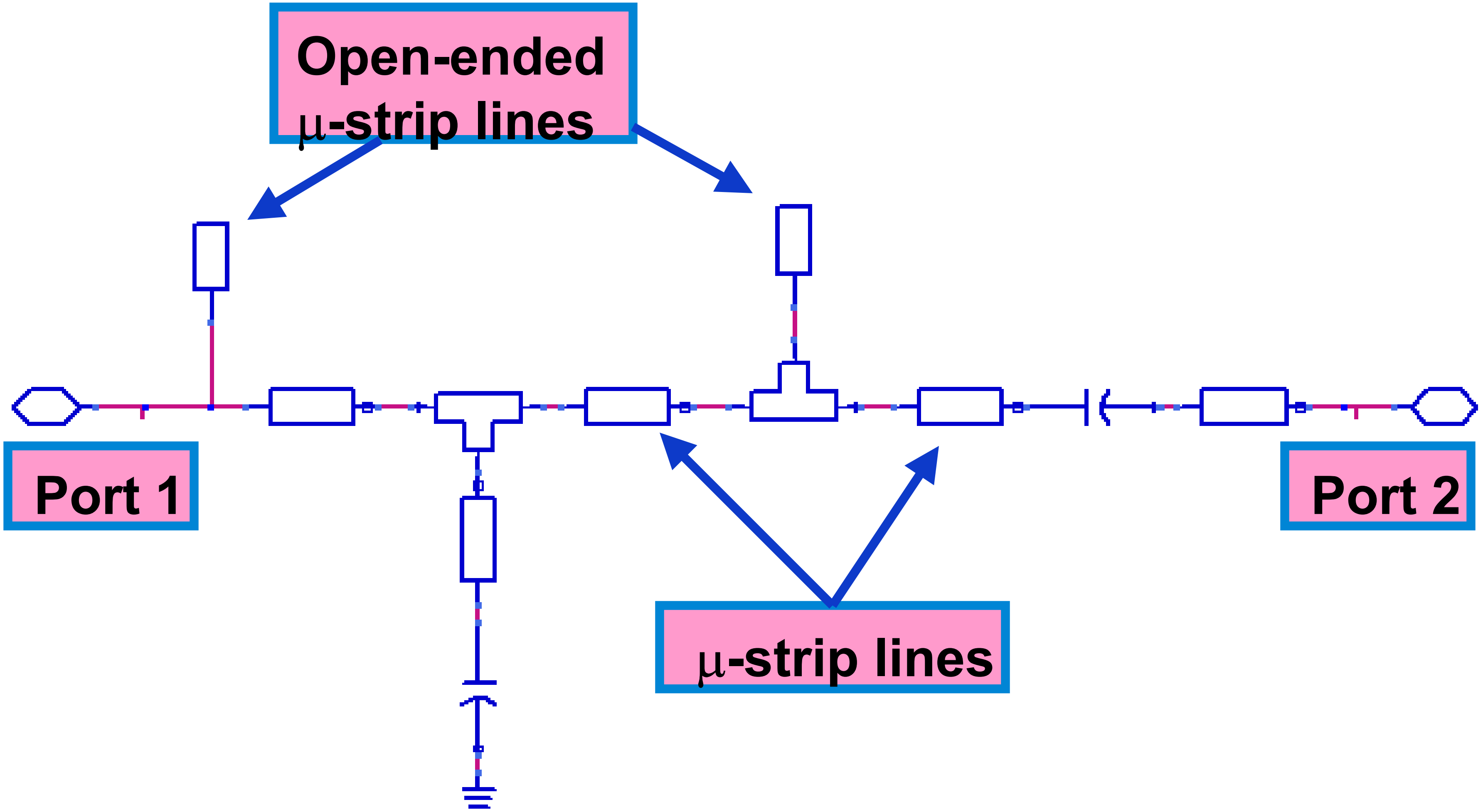
Interstage Matching Network



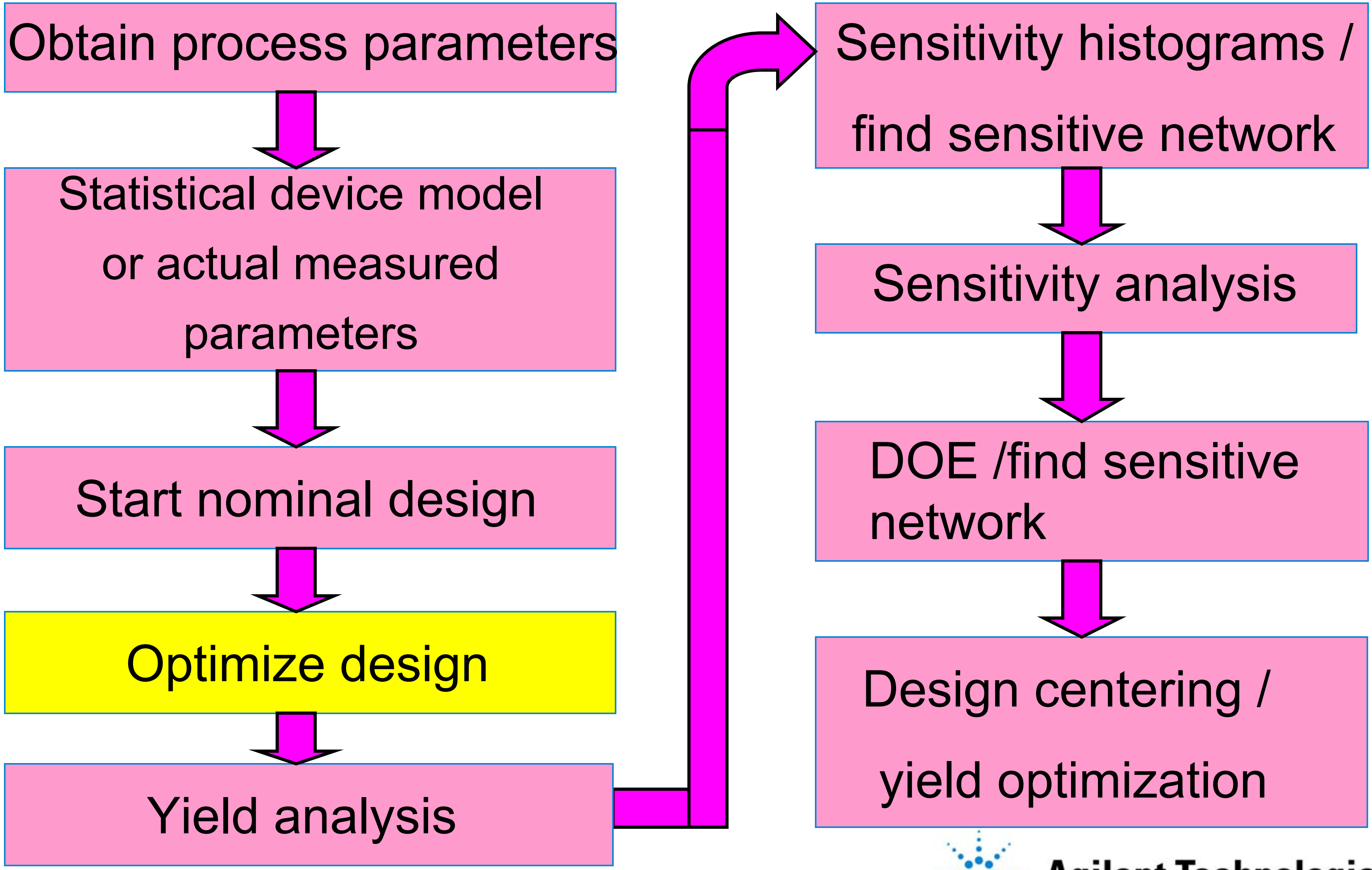
FET2 Structure with Stability Resistors



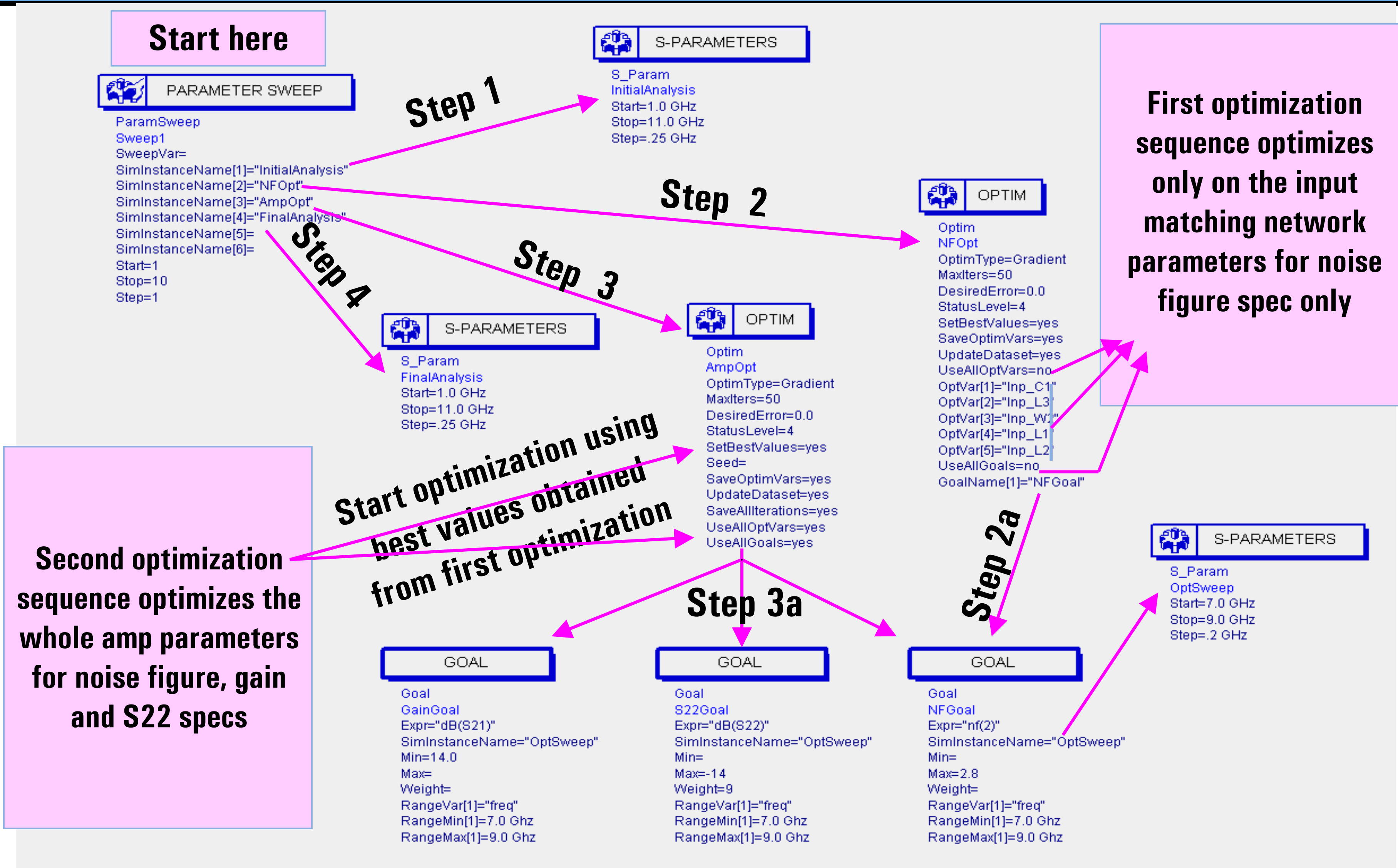
Output Matching Network



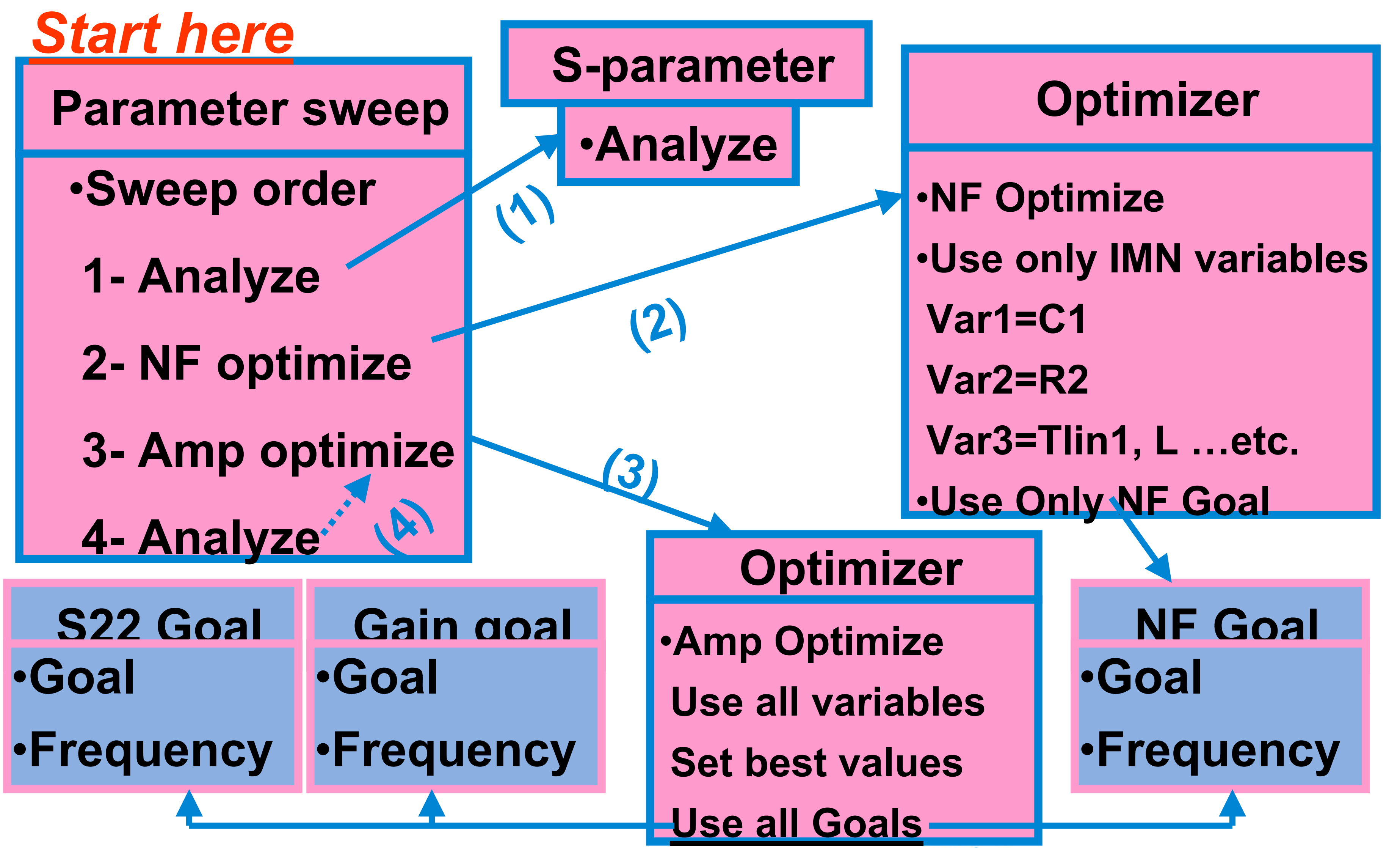
MMIC Statistical Design Process



Programmable Optimization Setup in ADS



Programmable Optimization Setup



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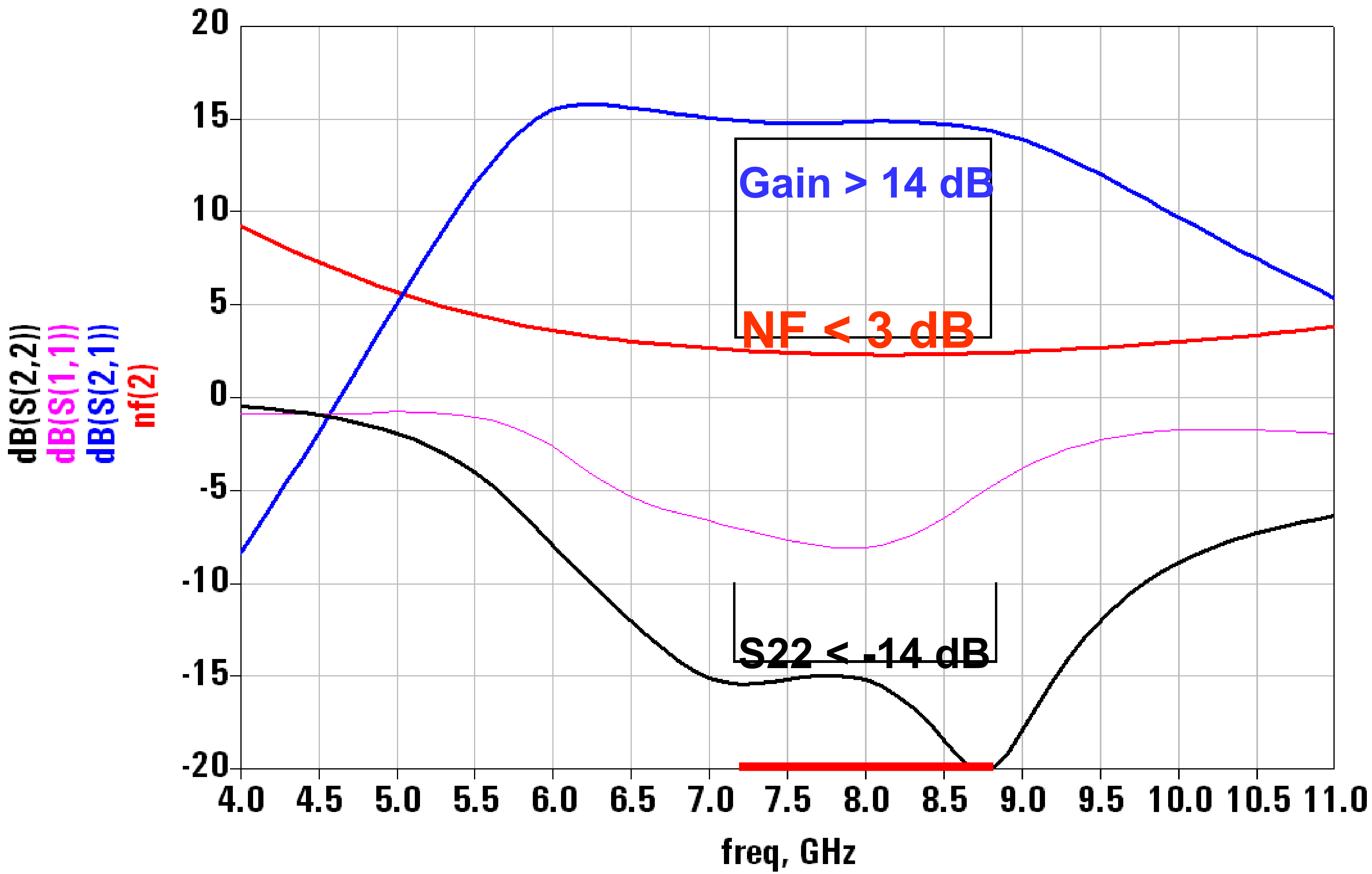
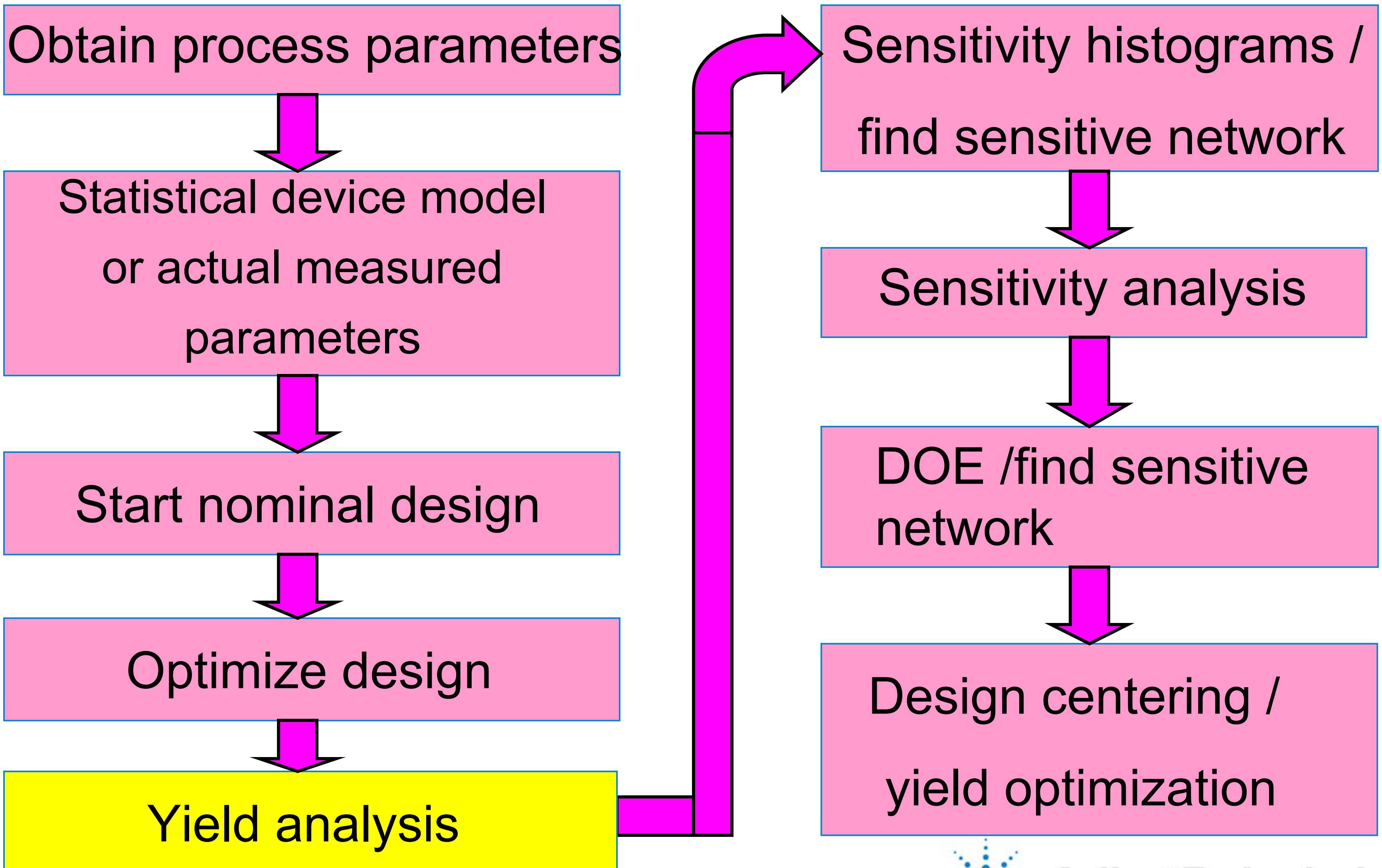
LNA Response after Optimization



MMIC Statistical Design Process



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Yield Analysis in ADS

YIELD
Yield
Yield1
NumIters=200
PPT_Mode=none
ShadowModelType=none
Seed=
SaveSolns=yes
SaveSpecs=yes
SaveRandVars=yes
UpdateDataset=no
SaveAllIterations=yes
UseAllSpecs=yes
StatusLevel=2

S-PARAMETERS
S_Param
YldSweep
Start=7.2 GHz
Stop=8.8 GHz
Step=.2 GHz

YIELD SPEC
YieldSpec
NF_Spec
Expr="max(nf(2))"
SimInstanceName="YldSweep"
Min=
Max=2.8
Weight=
Save=
RangeVar[1]=
RangeMin[1]=
RangeMax[1]=

YIELD SPEC
YieldSpec
Gain_Spec
Expr="min(dB(S21))"
SimInstanceName="YldSweep"
Min=14.0
Max=
Weight=
Save=
RangeVar[1]=
RangeMin[1]=
RangeMax[1]=

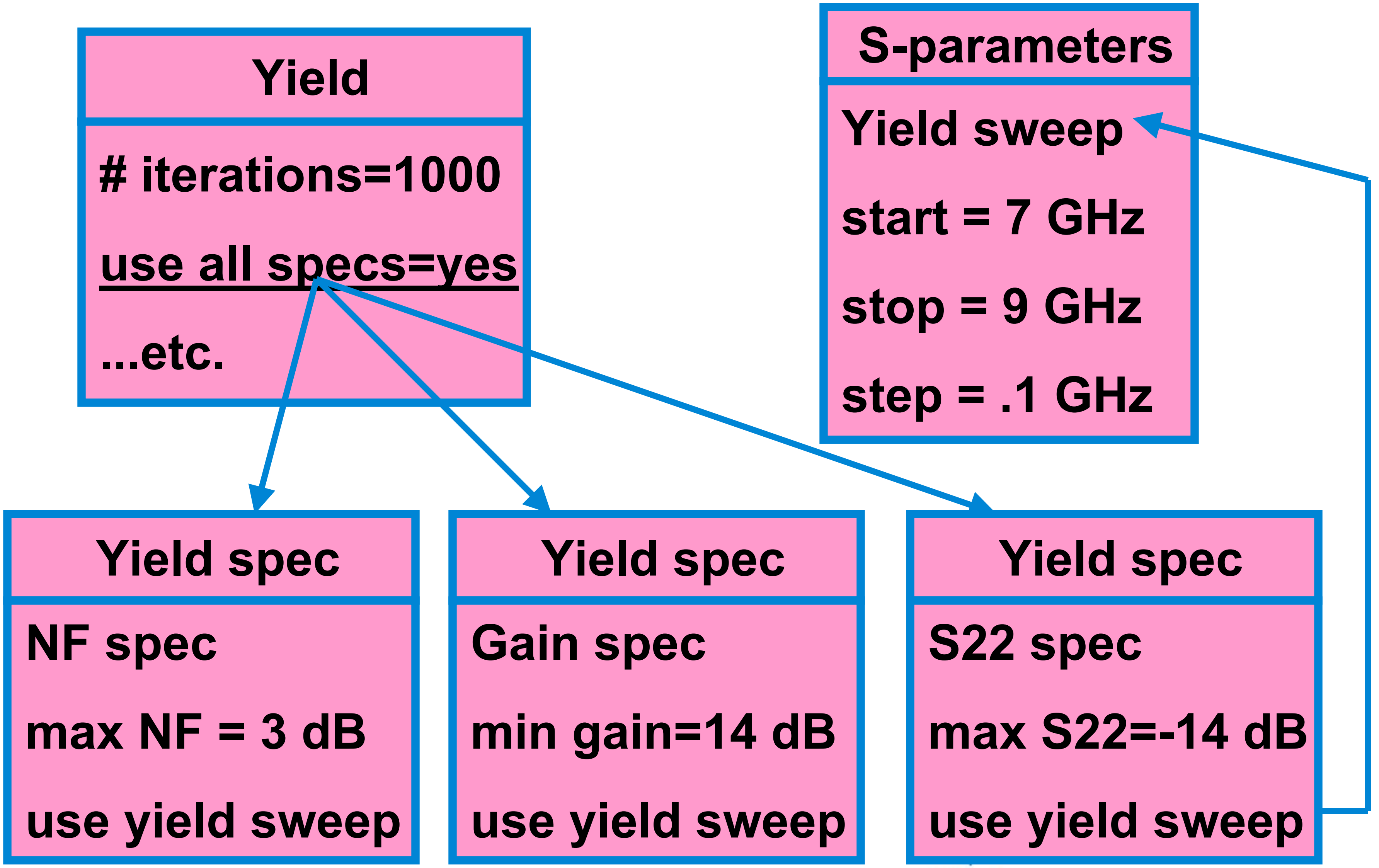
YIELD SPEC
YieldSpec
S22_Spec
Expr="max(dB(S22))"
SimInstanceName="YldSweep"
Min=
Max=-14
Weight=
Save=
RangeVar[1]=
RangeMin[1]=
RangeMax[1]=

VAR
VAR2
Inp_L2=17.2666 opt{ 10 to 100 }
Inp_L1=1064.12 opt{ 800 to 1300 }
Inp_W2=14.3175 opt{ 5 to 25 } stat{ uniform +/- .5 }
Inp_W3=5.75363 opt{ 5 to 25 } stat{ uniform +/- .5 }
Inp_L3=268.891 opt{ 100 to 550 }
Inp_C1=4.20706 opt{ .1 to 6 } stat{ uniform +/- 5 % }
Inp_R1=27.9732 opt{ 25 to 30 } stat{ uniform +/- 5 % }

VAR
VAR5
FET2_L1=261.487 opt{ 10 to 550 }
FET2_W1=10.0692 opt{ 5 to 50 } stat{ uniform +/- .5 }
FET2_W2=9.12953 opt{ 5 to 50 } stat{ uniform +/- .5 }
FET2_W4=10.2946 opt{ 5 to 50 } stat{ uniform +/- .5 }
FET2_W3=7.74289 opt{ 5 to 50 } stat{ uniform +/- .5 }
FET2_R1=29.3678 opt{ 25 to 30 } stat{ uniform +/- 5 % }
FET2_R2=20 opt{ 20 to 25 } stat{ uniform +/- 5 % }
FET2_R3=165.472 opt{ 150 to 200 } stat{ uniform +/- 5 % }
FET2_L2=176.628 opt{ 10 to 250 }
FET2_L3=24.7259 opt{ 2 to 250 }
FET2_L4=98.0301 opt{ 2 to 250 }

Page 17 has an easier-to-read diagram

Yield Analysis (Simplified Setup)

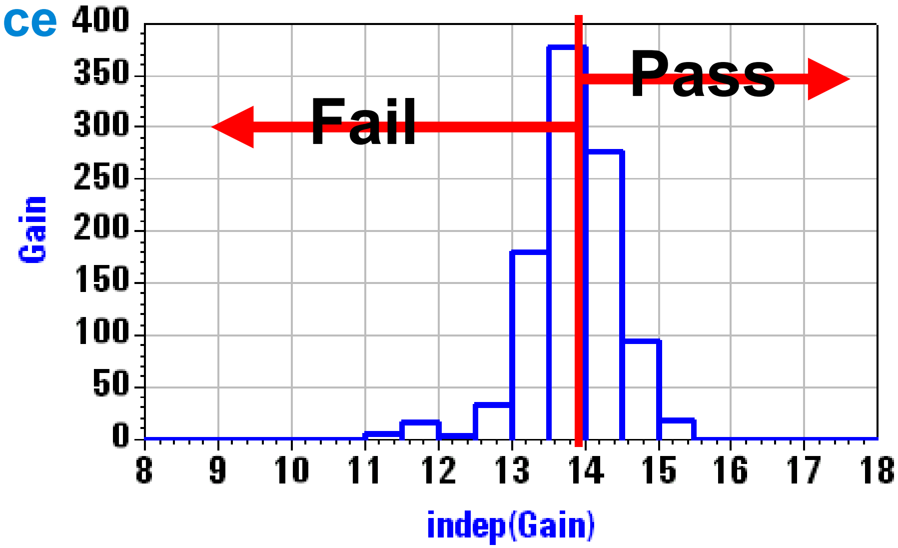


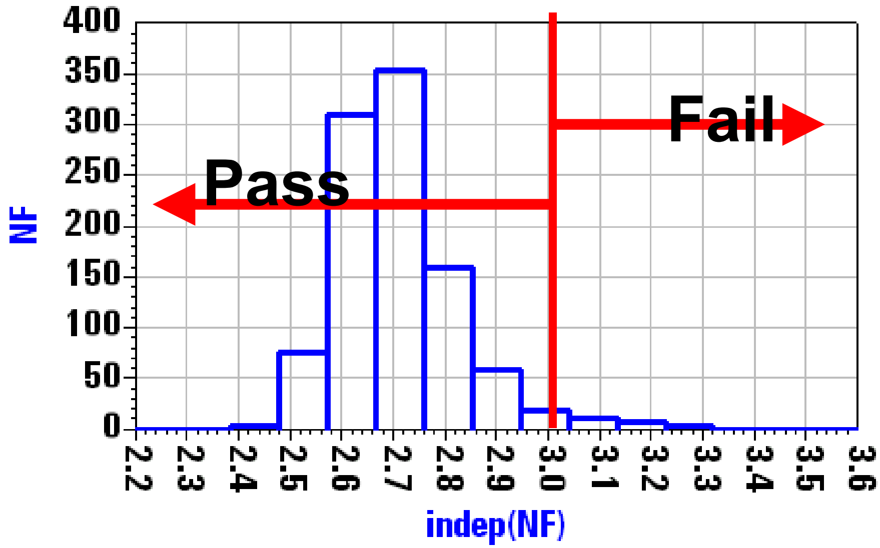
Yield after Optimization : 8.8 %

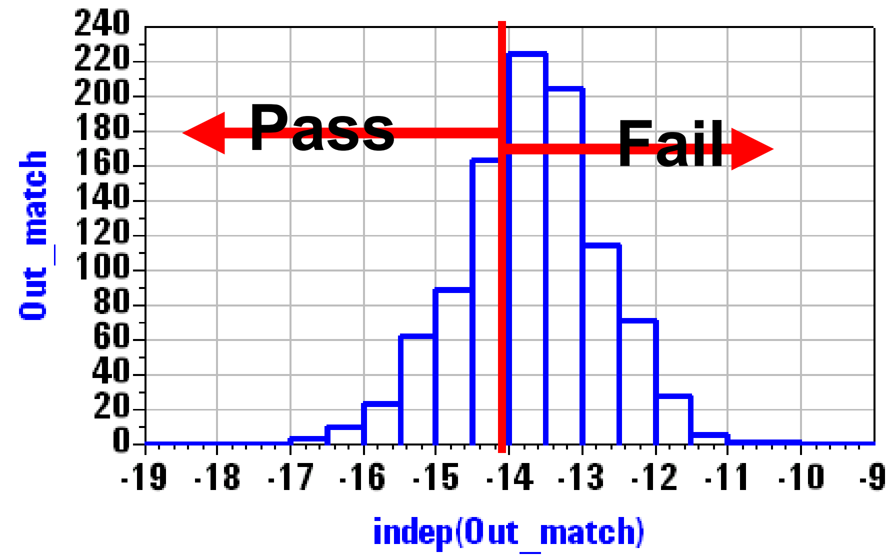
Statistical Analysis of LNA Performance

- 5% Gaussian variation in lumped
- Line widths vary ± 1/2 um
- Substrate height 100 um ± 3 um
- Substrate Er 12.9 ± 5%
- 42 FET samples

NumFail	NumPass	Yield
912.00	88.00	8.80







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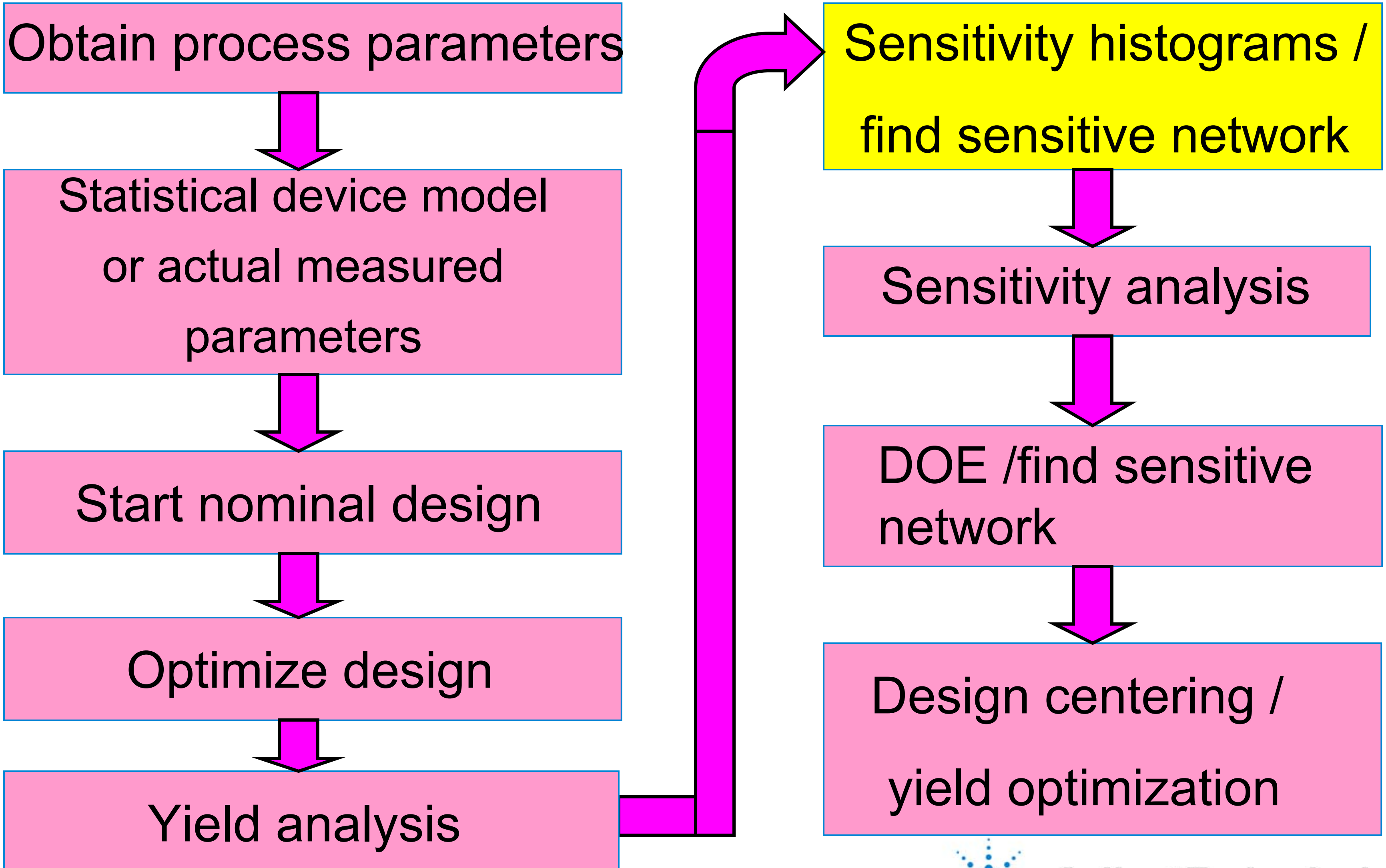
LNA Yield / Versus Variation in Each Section

Element name	Yield
Input matching network	100 %
Interstage matching network	100 %
Output matching network	70 %
FETs (42 samples)	25 %
Er (dielectric constant)	87 %
H (substrate height)	100 %
Overall yield (vary everything)	8.8 %

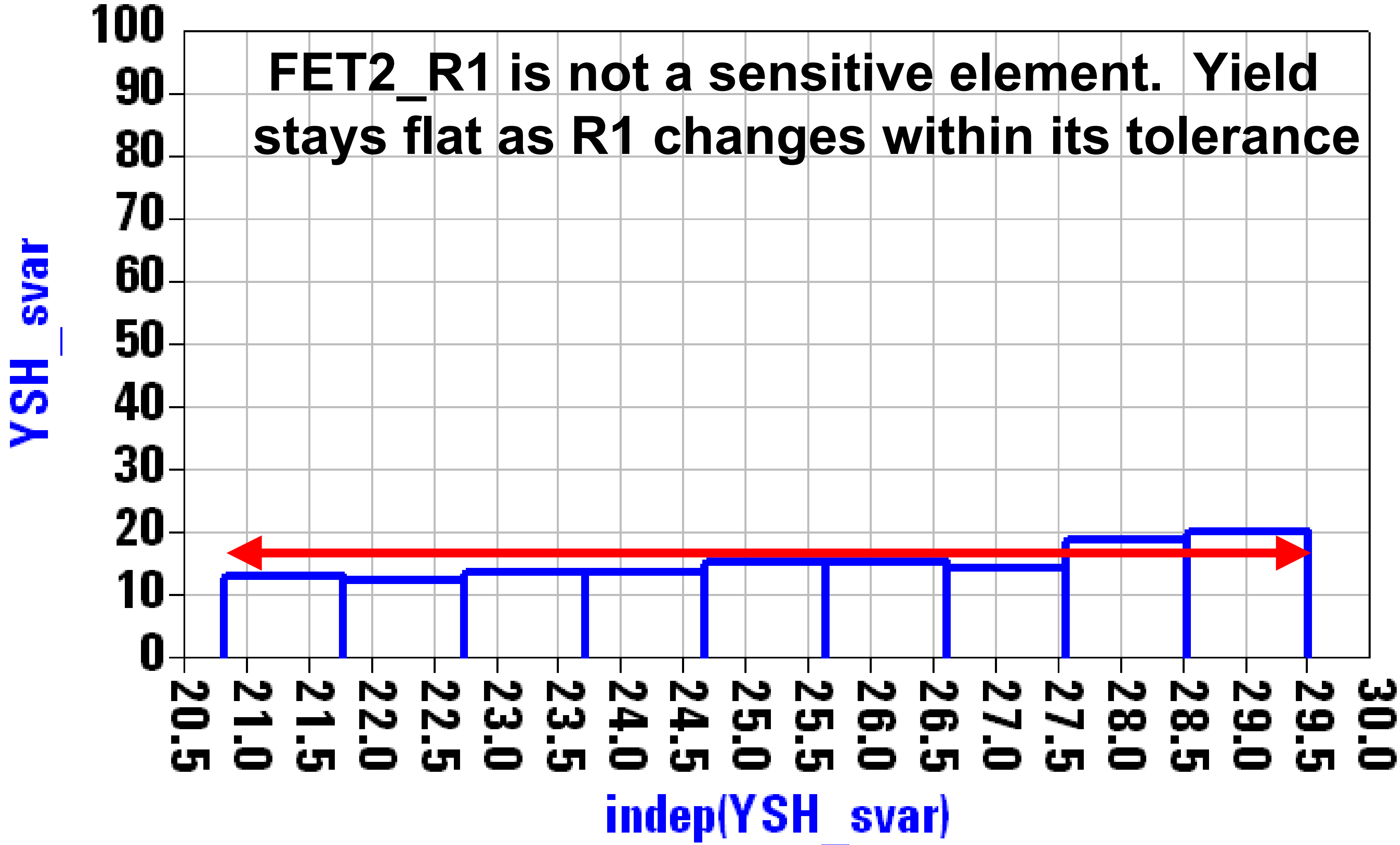
MMIC Statistical Design Process



Yield Sensitivity Histograms (YSH)

- Data that are stored from a yield analysis run are post processed via built-in AEL Expressions to extract and display results
- YSH display yield with respect to each element variation.
- YSH provide insight to how sensitive the design specs are with respect to each of the design's elements.
- YSH help designers to pinpoint the sensitive parts in their designs. As a result, designers make decision to replace these parts with "tighter tolerance parts" in Board application (OR) create "less sensitive matching networks" in IC designs.
- YSH also allow designers to manually adjust the nominal values of design elements in order to increase the yield.

Yield Sensitivity with Respect to FET2_R1



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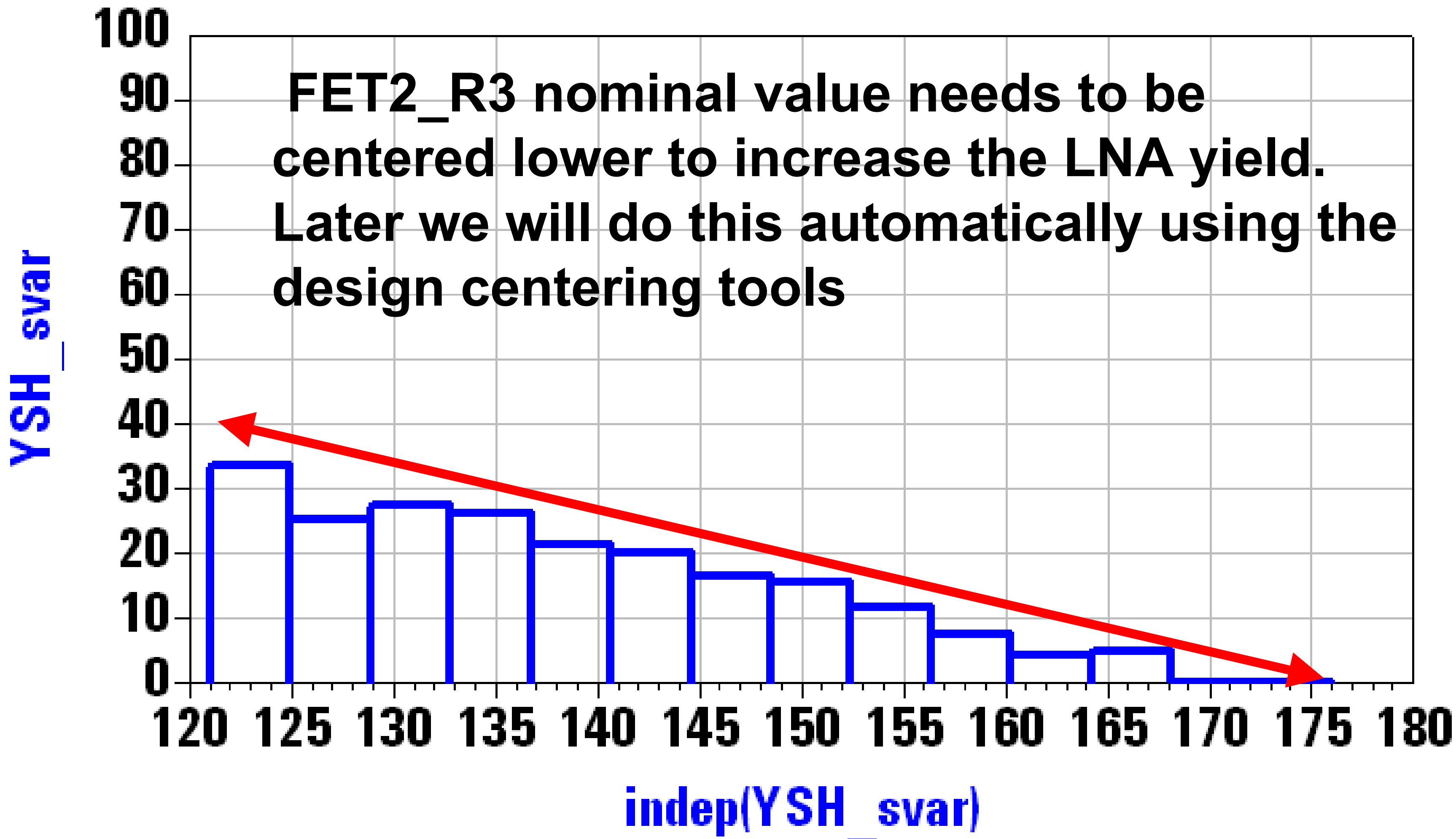
Yield Sensitivity with Respect to FET2_R3



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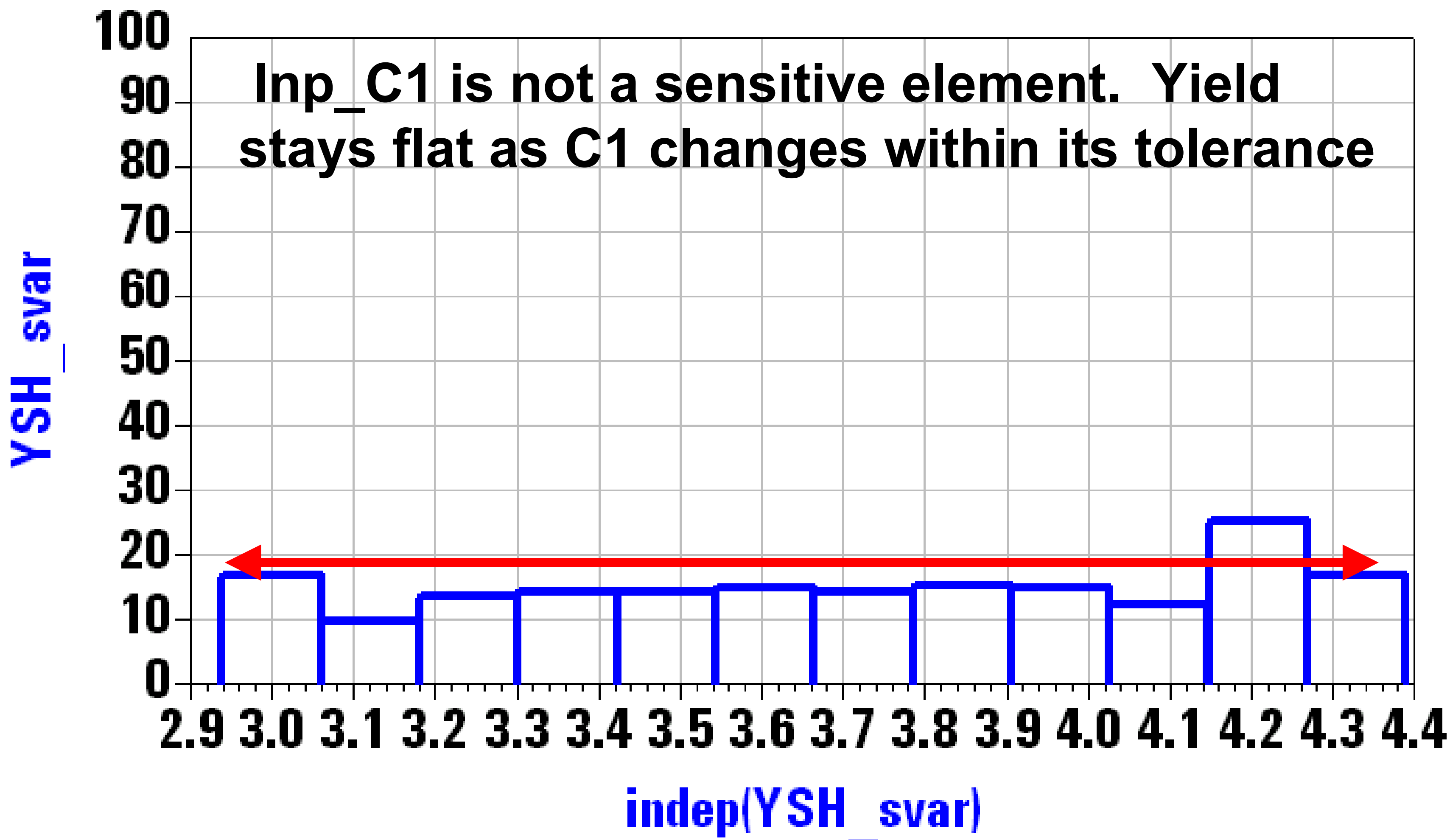
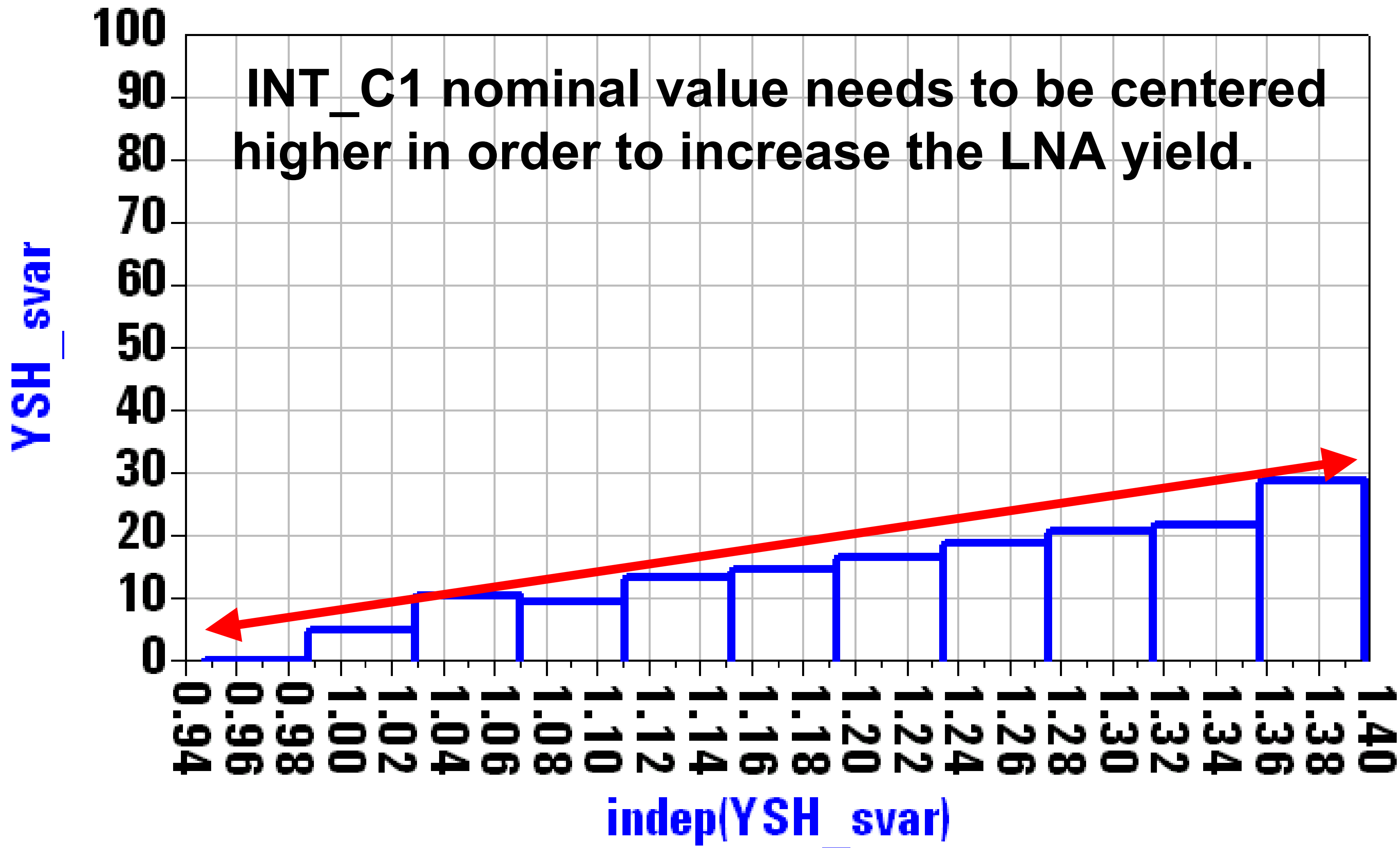
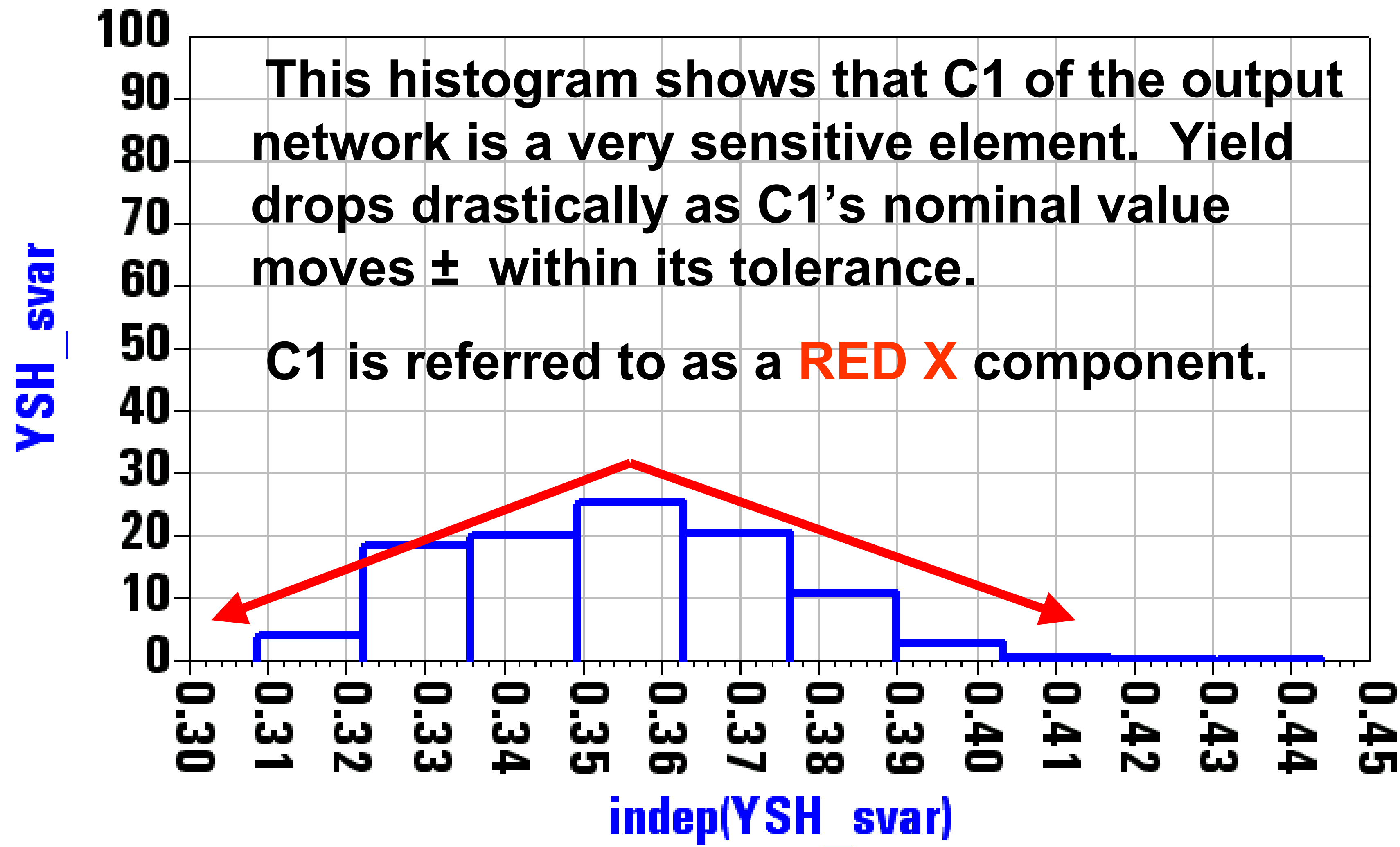
Yield Sensitivity with Respect to Inp_C1



Yield Sensitivity with Respect to INT_C1



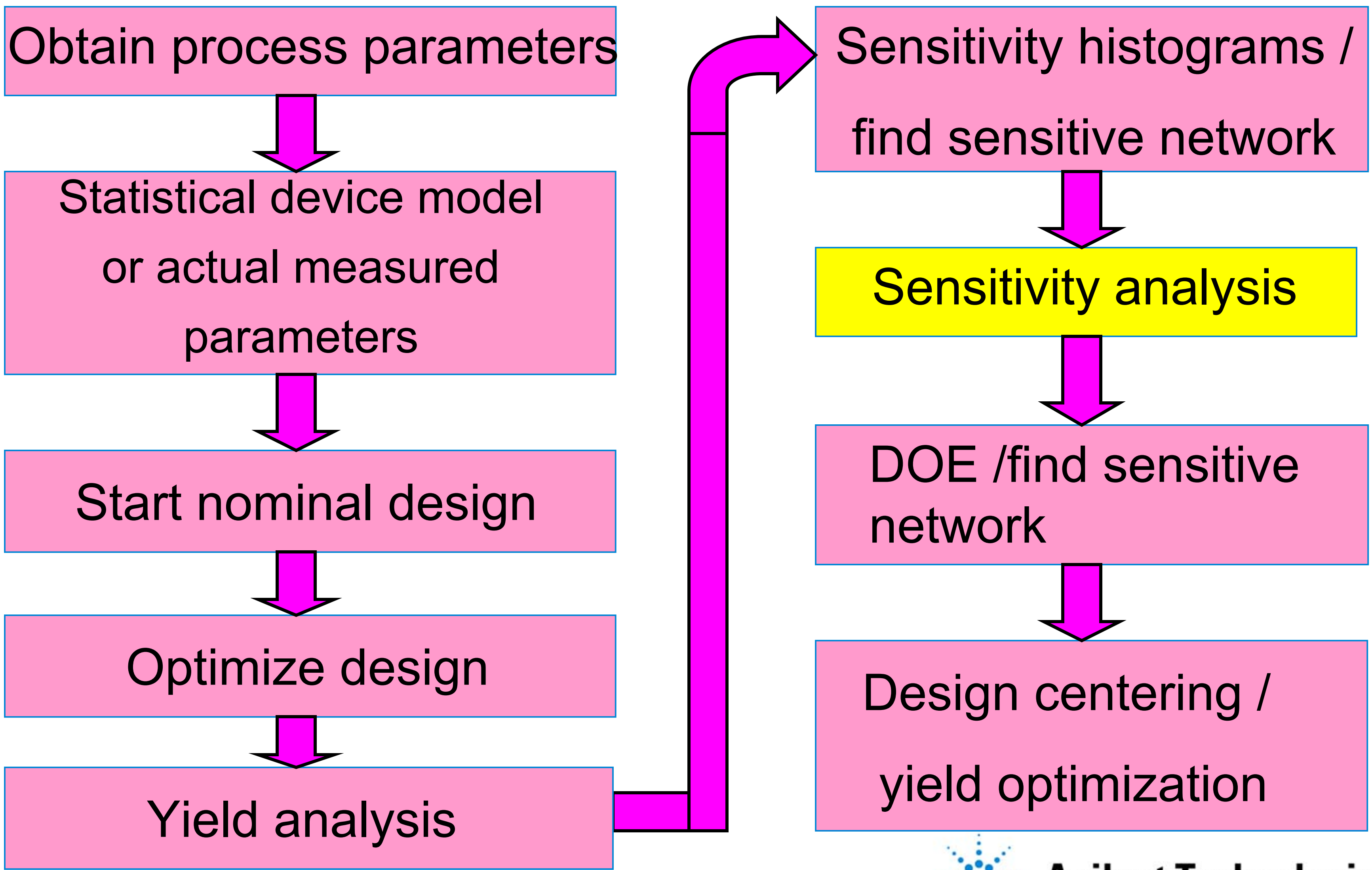
Yield Sensitivity with Respect to OUT_C1



Break for Questions and Answers

Q & A

MMIC Statistical Design Process



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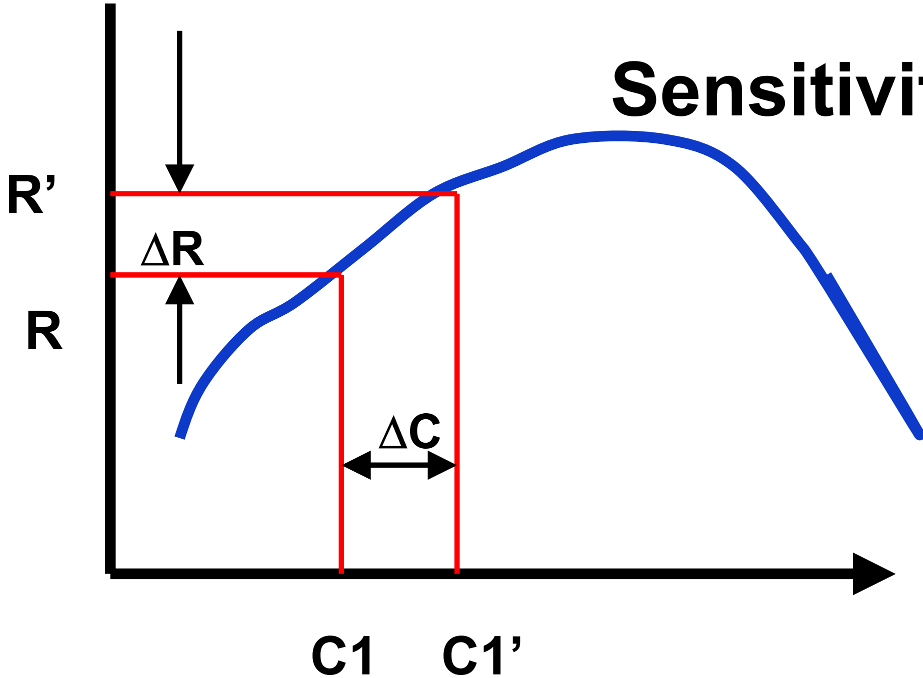
Sensitivity Analysis – How Does it Work?

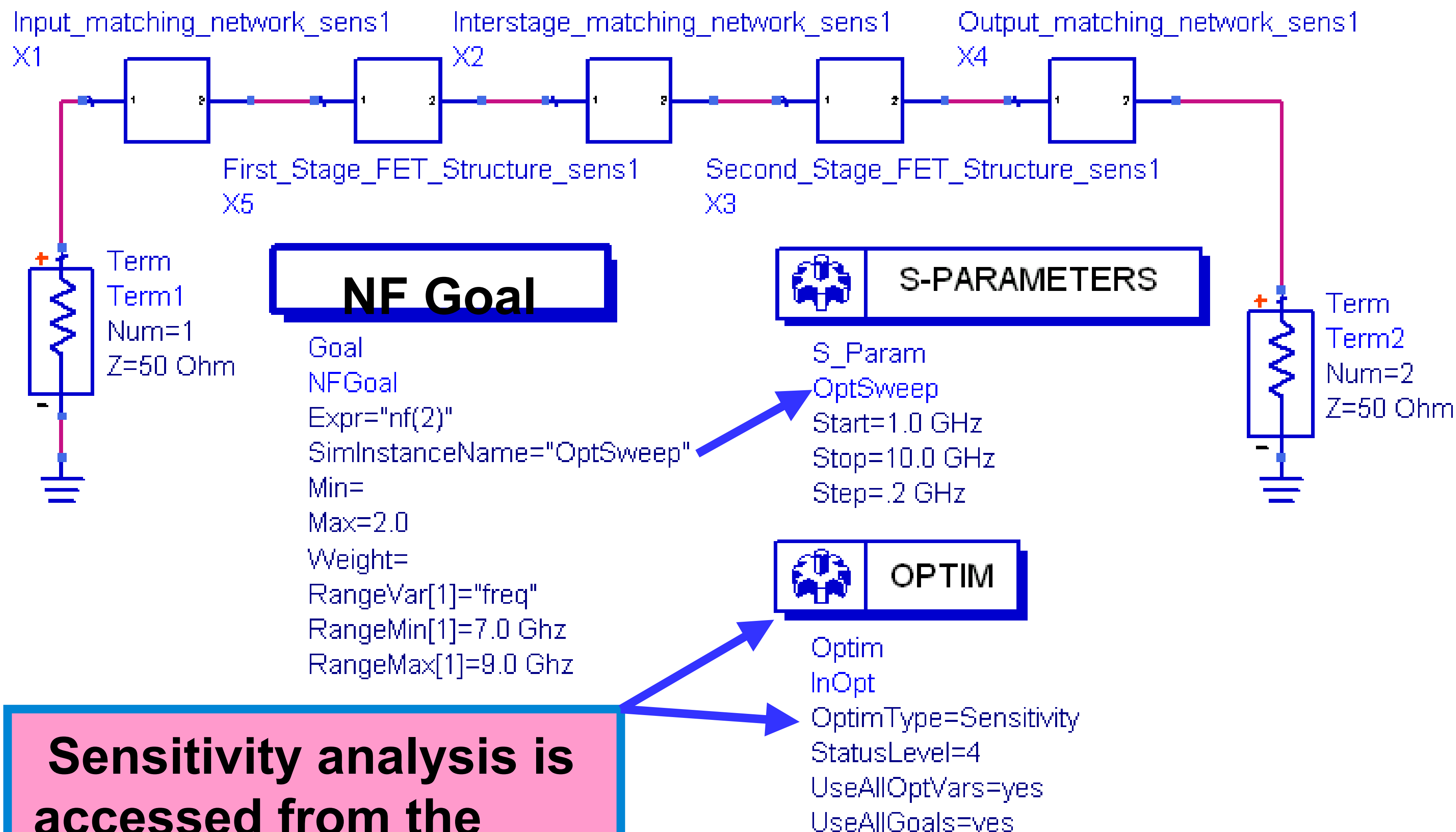
- Change the part's nominal value by 1e-6 and monitor the change in the response (R).
- Example for capacitor, C1 with response R
- Perturb C1 by a small delta: C1' = C1(1+1e-6)



Sensitivity analysis is local. It changes one part at a time.

YSH has wider variation and changes all parts together.

Sensitivity Analysis to NF Setup



Sensitivity analysis is accessed from the optimization controller

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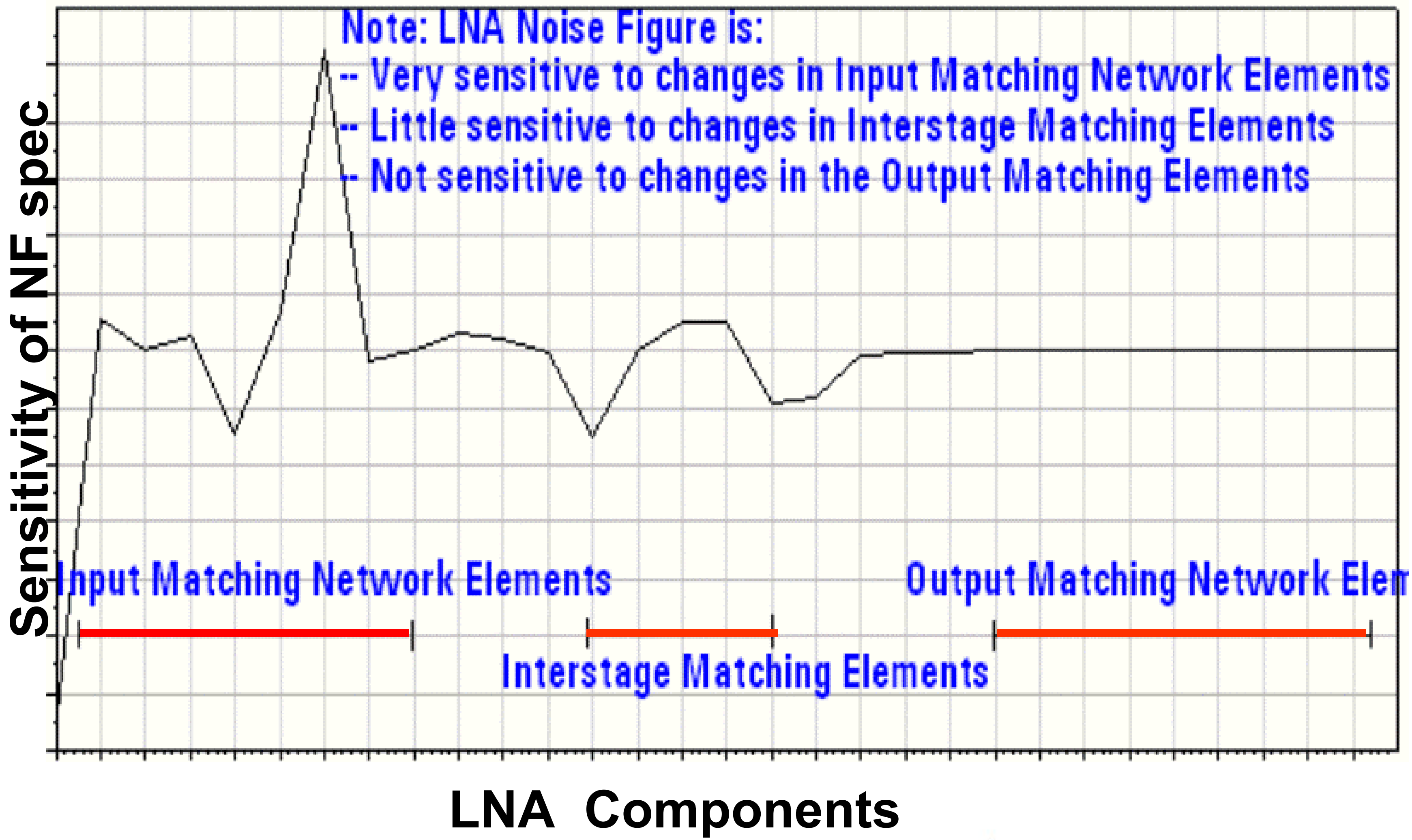
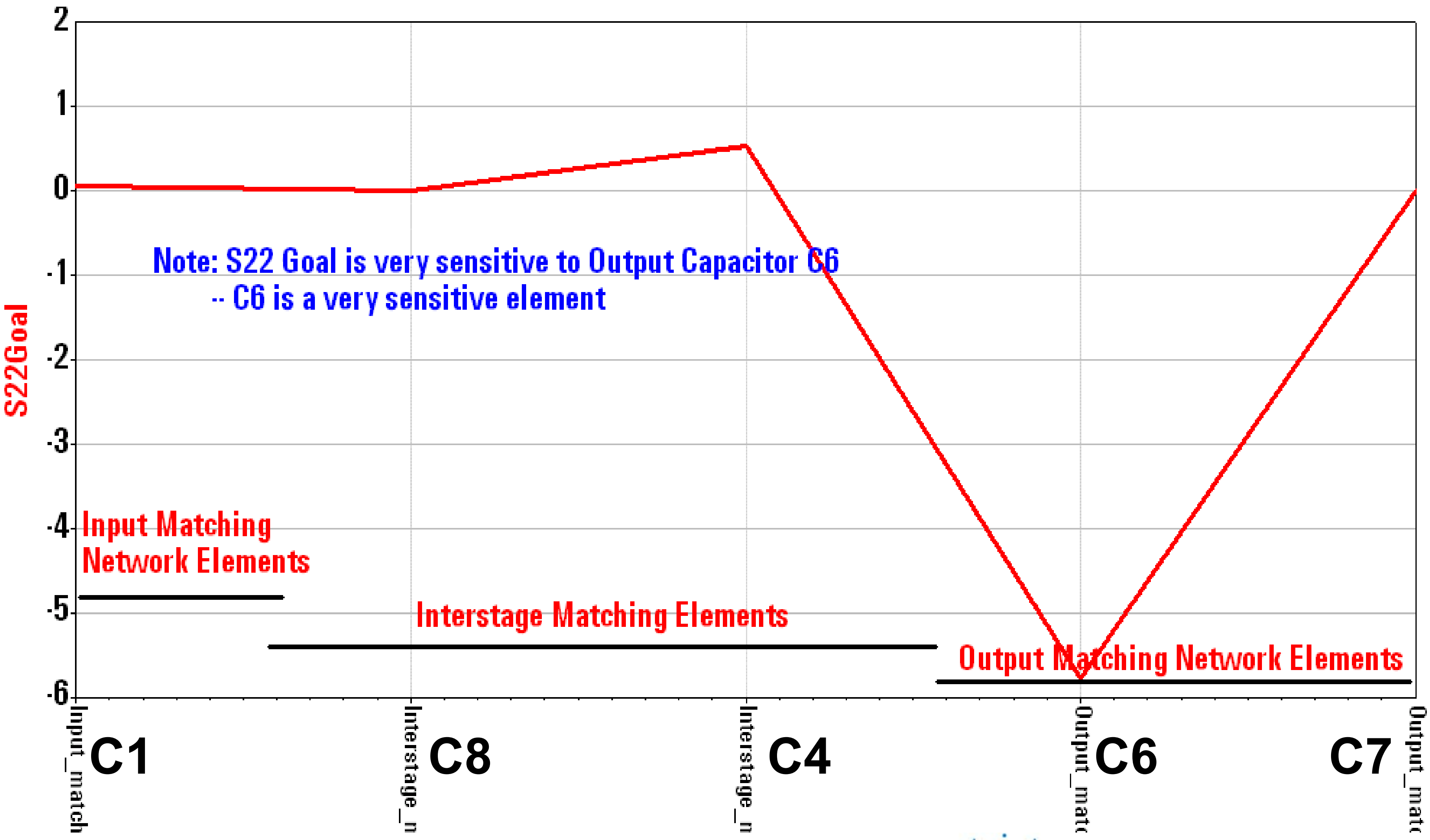
Sensitivity Analysis to NF Spec



Sensitivity Analysis to S22 Spec



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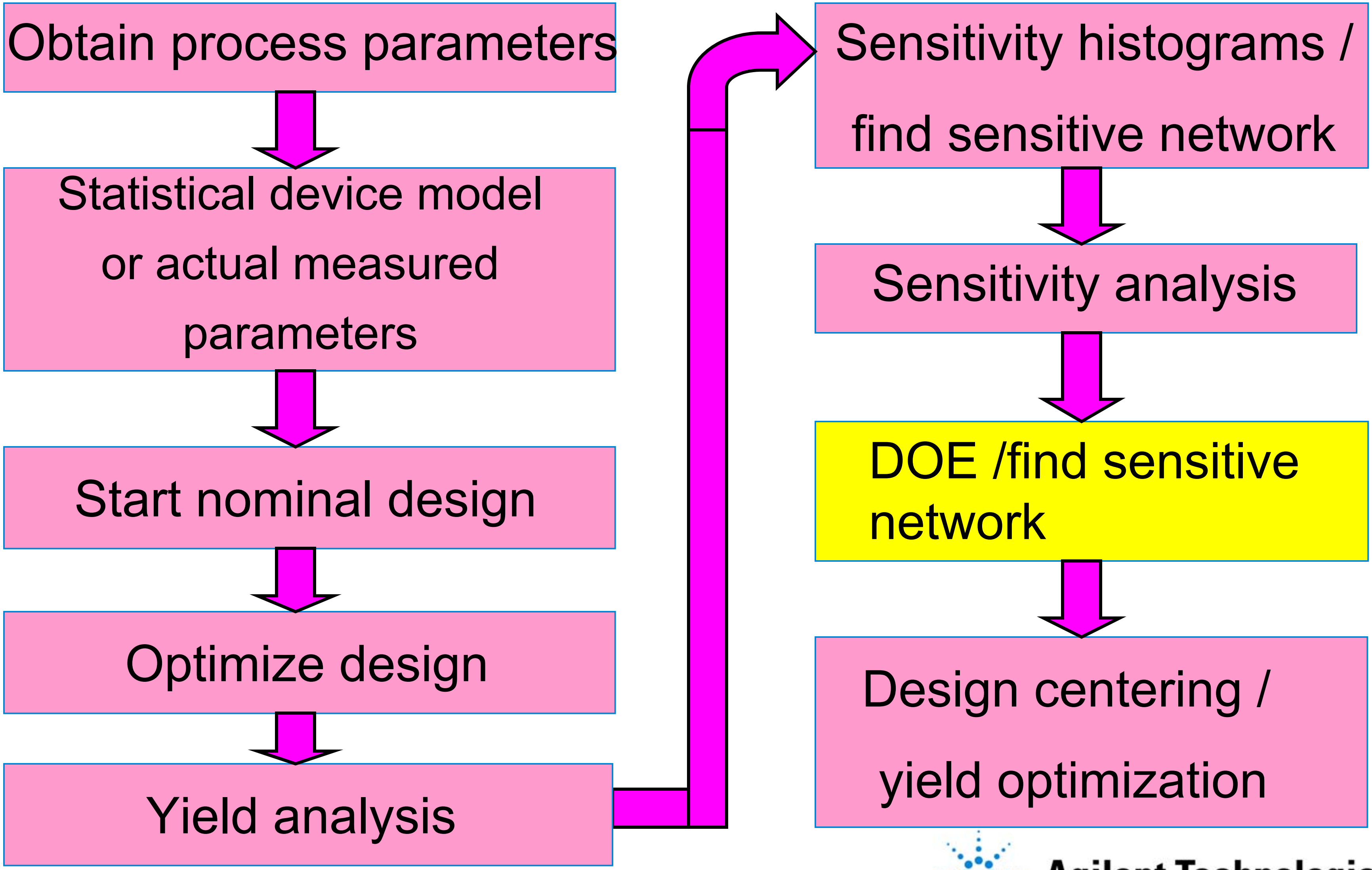
MMIC Statistical Design Process



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Design of Experiments (DOE) on the LNA

- Lump all input matching network elements together and vary them with a steering variable (d_inp) ± 5%
- Do the same with the interstage and output
- DOE variables are then d_inp, d_int, and d_out
- This should provide us with more information on the sensitivity of the matching networks.
- The 3 variables require 8 simulation runs = (2^3)

How Does Steering Variable d_inp Work ?

Example:

For input matching network variables C1, R1, W1

Set the following variables:

C1 = 5 pF * (1+d_inp)

R1 = 20 ohm * (1+d_inp)

W1 = 10 um * (1+d_inp)

d_inp = 0 DOE(± 5%)

d_inp steers all "input matching variables" as it changes from -5% to +5% for the DOE

Input and Output Variables of DOE

Get the output values at center frequency (8 GHz), or use the worst response across the frequency band

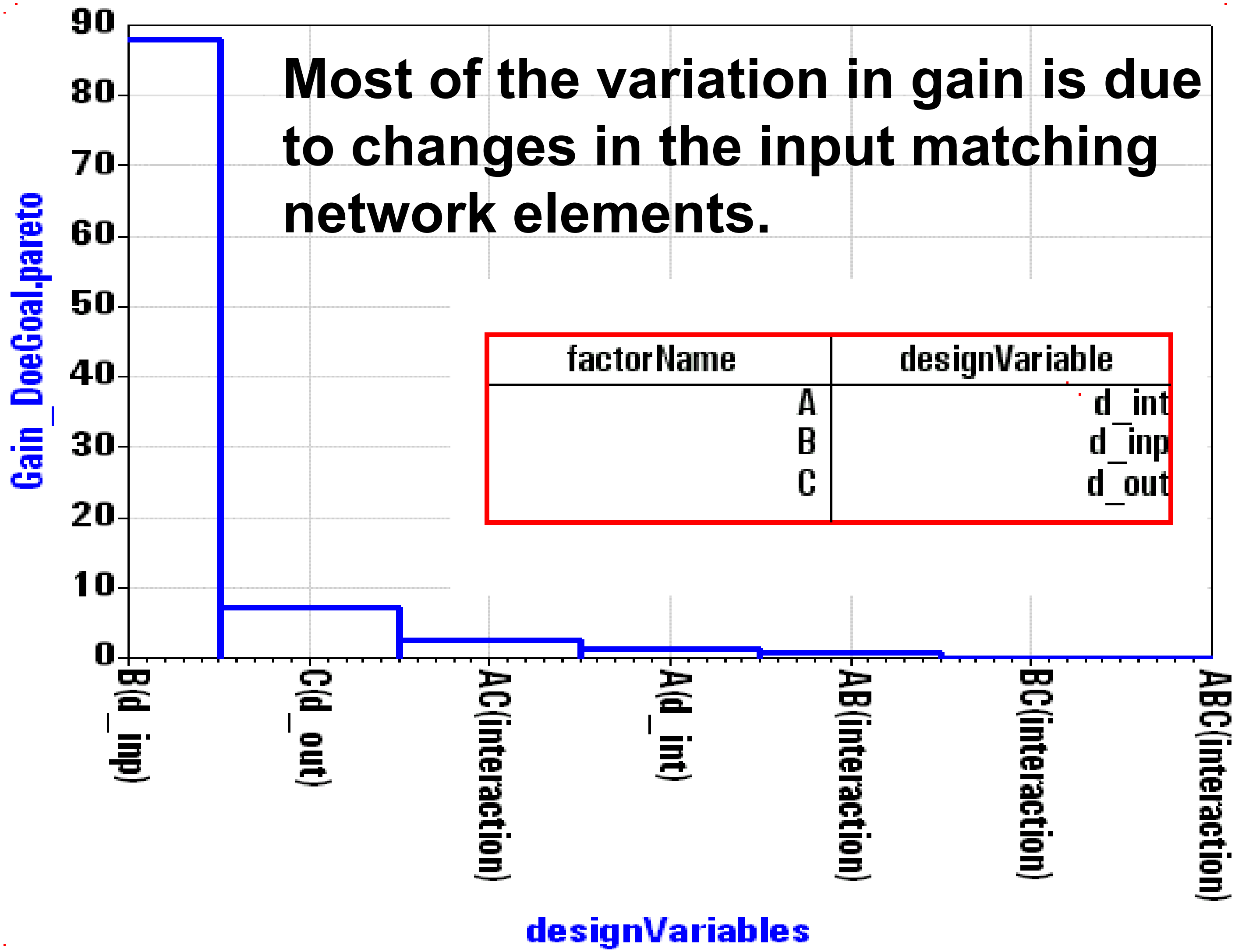
d_inp	d_int	d_out	Gain	NF	S22
1	1	1			
1	1	-1			
1	-1	1			
1	-1	-1			
-1	1	1			
-1	1	-1			
-1	-1	1			
-1	-1	-1			

DOE Results on Gain

Nominal Response

freq	dB(S(2,1))								
	doelter=0	doelter=1	doelter=2	doelter=3	doelter=4	doelter=5	doelter=6	doelter=7	doelter=8
7.200GHz	14.889	15.861	14.577	15.649	14.930	15.876	14.613	15.656	15.301
7.300GHz	14.809	15.834	14.521	15.634	14.820	15.822	14.528	15.616	15.241
7.400GHz	14.756	15.824	14.480	15.628	14.743	15.794	14.463	15.593	15.199
7.500GHz	14.712	15.820	14.451	15.627	14.682	15.778	14.418	15.582	15.172
7.600GHz	14.682	15.822	14.438	15.632	14.642	15.775	14.396	15.583	15.159
7.700GHz	14.669	15.829	14.436	15.637	14.624	15.782	14.391	15.590	15.159
7.800GHz	14.670	15.836	14.445	15.638	14.626	15.794	14.401	15.596	15.170
7.900GHz	14.680	15.835	14.463	15.630	14.640	15.800	14.424	15.596	15.187
8.000GHz	14.702	15.826	14.492	15.614	14.669	15.800	14.460	15.588	15.204
8.100GHz	14.691	15.756	14.485	15.532	14.668	15.736	14.463	15.513	15.178
8.200GHz	14.682	15.663	14.478	15.431	14.668	15.648	14.466	15.415	15.135
8.300GHz	14.662	15.535	14.456	15.289	14.658	15.520	14.452	15.271	15.076
8.400GHz	14.631	15.373	14.423	15.116	14.633	15.351	14.424	15.090	14.984
8.500GHz	14.581	15.169	14.374	14.910	14.585	15.133	14.376	14.870	14.864
8.600GHz	14.515	14.932	14.300	14.662	14.516	14.877	14.298	14.601	14.708
8.700GHz	14.419	14.651	14.198	14.375	14.410	14.569	14.185	14.288	14.507
8.800GHz	14.286	14.324	14.063	14.051	14.261	14.212	14.032	13.932	14.267

DOE Pareto Chart (Effects on Gain)



factorName	designVariable
A	d_int
B	d_inp
C	d_out

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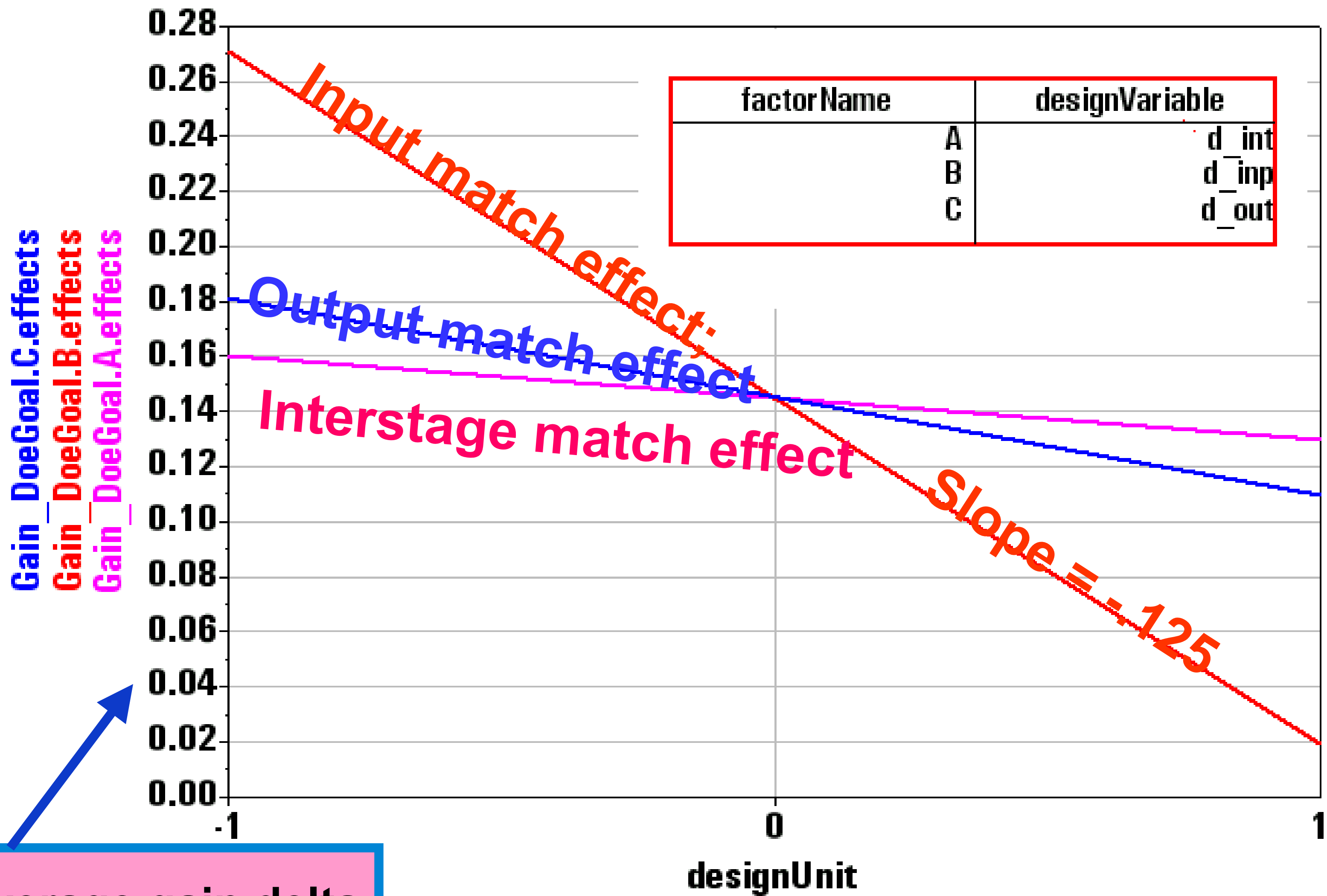
DOE Effects of Inp, Int, and Out on Gain



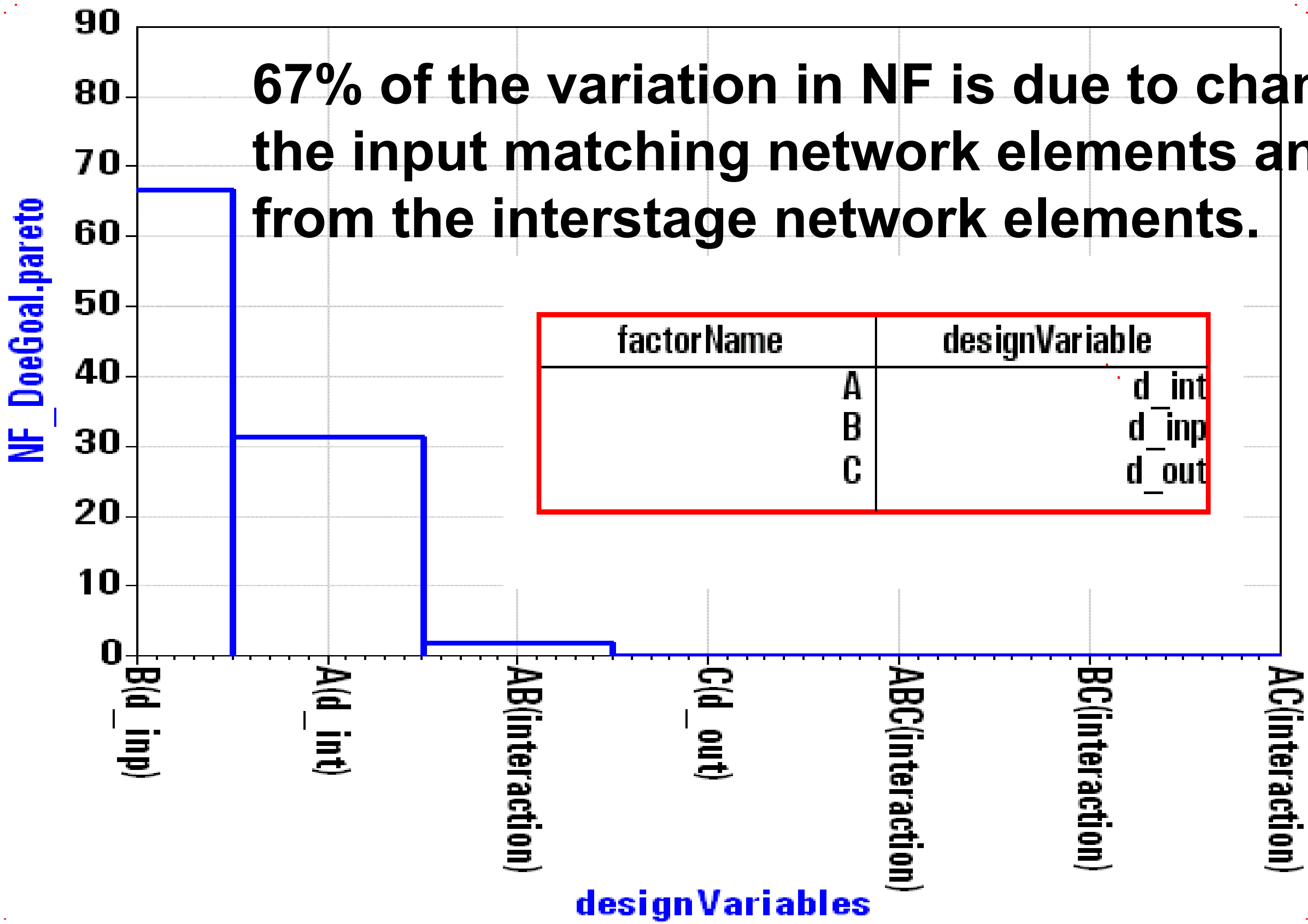
Average gain delta response from the 14 dB spec

DOE Results on NF

freq	nf(2)								
	doelter=0	doelter=1	doelter=2	doelter=3	doelter=4	doelter=5	doelter=6	doelter=7	doelter=8
7.200GHz	2.548	2.500	2.455	2.392	2.545	2.498	2.452	2.389	2.463
7.300GHz	2.499	2.444	2.420	2.349	2.497	2.442	2.417	2.347	2.419
7.400GHz	2.460	2.397	2.391	2.312	2.457	2.395	2.388	2.310	2.379
7.500GHz	2.422	2.352	2.366	2.278	2.420	2.350	2.363	2.276	2.344
7.600GHz	2.390	2.311	2.346	2.250	2.387	2.309	2.343	2.248	2.313
7.700GHz	2.363	2.275	2.330	2.226	2.360	2.274	2.328	2.225	2.288
7.800GHz	2.341	2.246	2.320	2.207	2.339	2.245	2.317	2.206	2.268
7.900GHz	2.325	2.221	2.314	2.193	2.323	2.220	2.312	2.193	2.253
8.000GHz	2.314	2.202	2.312	2.185	2.312	2.202	2.311	2.185	2.244
8.100GHz	2.310	2.191	2.316	2.183	2.308	2.190	2.315	2.183	2.240
8.200GHz	2.311	2.185	2.324	2.185	2.310	2.186	2.323	2.186	2.242
8.300GHz	2.317	2.187	2.338	2.194	2.317	2.187	2.337	2.195	2.249
8.400GHz	2.330	2.194	2.356	2.208	2.329	2.195	2.355	2.210	2.263
8.500GHz	2.347	2.208	2.377	2.228	2.347	2.210	2.377	2.230	2.281
8.600GHz	2.369	2.228	2.403	2.253	2.370	2.230	2.404	2.255	2.304
8.700GHz	2.396	2.254	2.434	2.284	2.397	2.257	2.435	2.286	2.334
8.800GHz	2.429	2.287	2.469	2.320	2.430	2.290	2.471	2.323	2.368

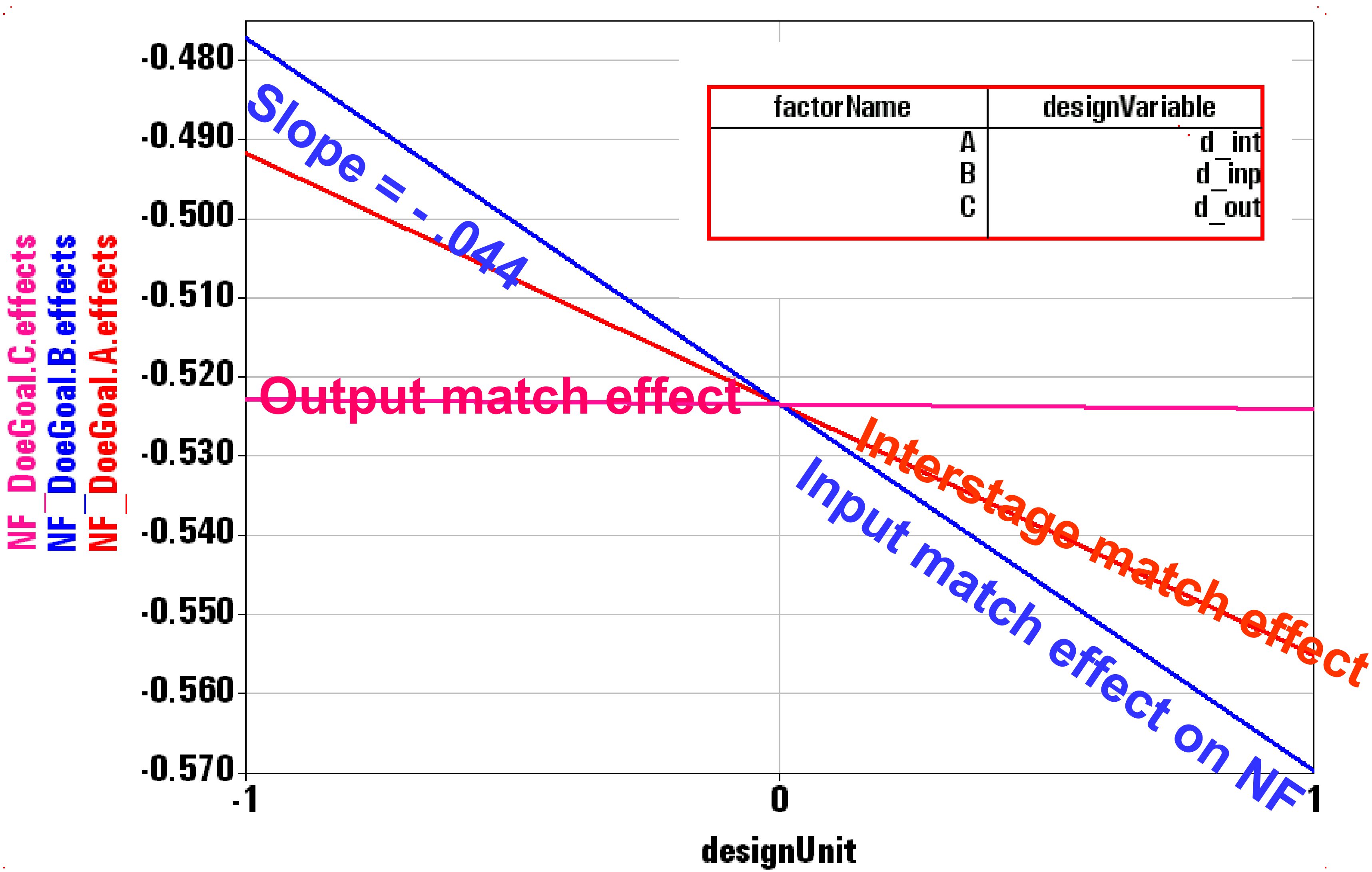
DOE Pareto of Effects on NF

67% of the variation in NF is due to changes in the input matching network elements and 31% from the interstage network elements.



factorName	designVariable
A	d_int
B	d_inp
C	d_out

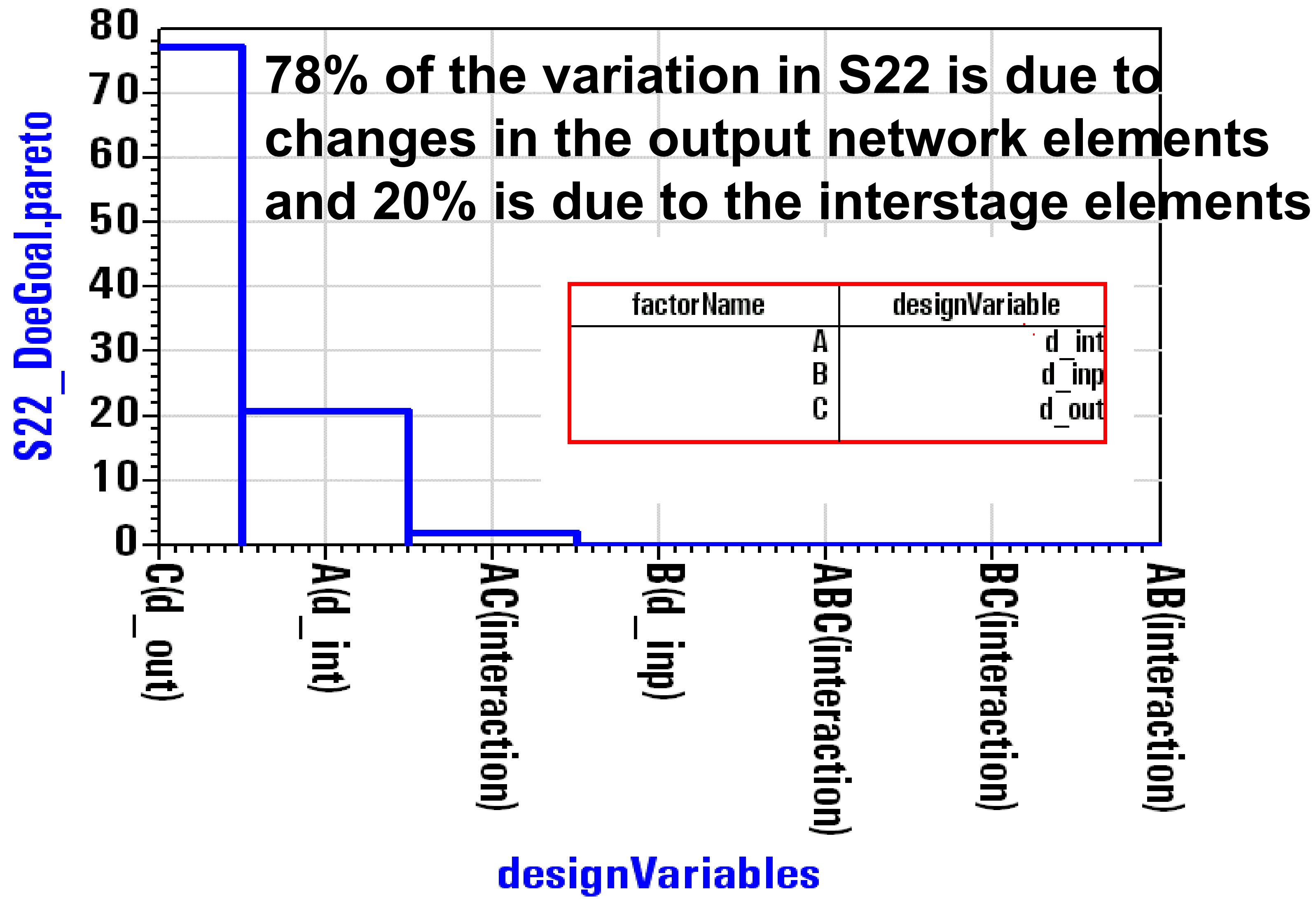
DOE Effects of Inp, Int, and Out on NF



DOE Results on S22

freq	dB(S(2,2))								
	doelter=0	doelter=1	doelter=2	doelter=3	doelter=4	doelter=5	doelter=6	doelter=7	doelter=8
7.200GHz	-14.187	-16.167	-14.117	-16.219	-12.094	-12.947	-11.905	-12.777	-14.013
7.300GHz	-14.645	-16.784	-14.582	-16.819	-11.926	-12.820	-11.771	-12.692	-13.956
7.400GHz	-14.957	-17.152	-14.903	-17.173	-11.790	-12.749	-11.667	-12.668	-13.866
7.500GHz	-15.134	-17.297	-15.088	-17.297	-11.695	-12.757	-11.606	-12.724	-13.777
7.600GHz	-15.196	-17.262	-15.156	-17.243	-11.654	-12.860	-11.598	-12.876	-13.719
7.700GHz	-15.175	-17.121	-15.148	-17.098	-11.677	-13.079	-11.656	-13.149	-13.716
7.800GHz	-15.114	-16.948	-15.105	-16.937	-11.776	-13.436	-11.793	-13.571	-13.788
7.900GHz	-15.054	-16.809	-15.066	-16.814	-11.970	-13.975	-12.026	-14.178	-13.961
8.000GHz	-15.023	-16.730	-15.056	-16.753	-12.271	-14.726	-12.367	-15.001	-14.256
8.100GHz	-15.087	-16.830	-15.149	-16.880	-12.718	-15.777	-12.862	-16.148	-14.725
8.200GHz	-15.240	-17.040	-15.329	-17.107	-13.323	-17.187	-13.516	-17.660	-15.387
8.300GHz	-15.512	-17.362	-15.640	-17.450	-14.139	-19.117	-14.403	-19.750	-16.261
8.400GHz	-15.918	-17.752	-16.082	-17.841	-15.225	-21.756	-15.570	-22.561	-17.425
8.500GHz	-16.481	-18.147	-16.669	-18.204	-16.689	-25.163	-17.124	-25.886	-18.893
8.600GHz	-17.193	-18.417	-17.422	-18.441	-18.676	-27.061	-19.279	-26.729	-20.663
8.700GHz	-18.069	-18.456	-18.325	-18.430	-21.569	-24.293	-22.443	-23.515	-22.493
8.800GHz	-19.063	-18.175	-19.315	-18.103	-26.232	-20.746	-27.641	-20.186	-23.413

DOE Pareto of Effects on S22



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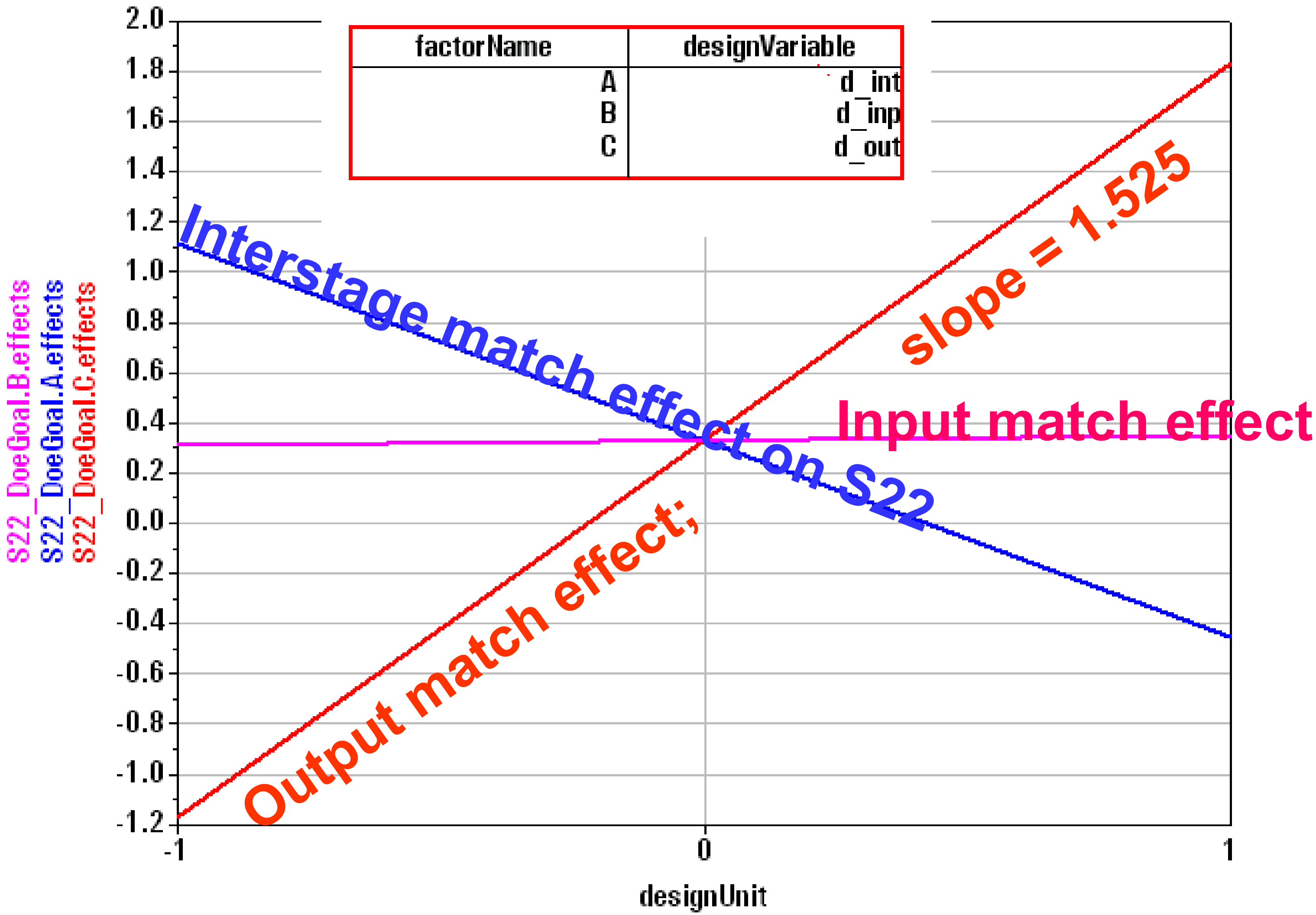
DOE Effects of Inp, Int, and Out on S22

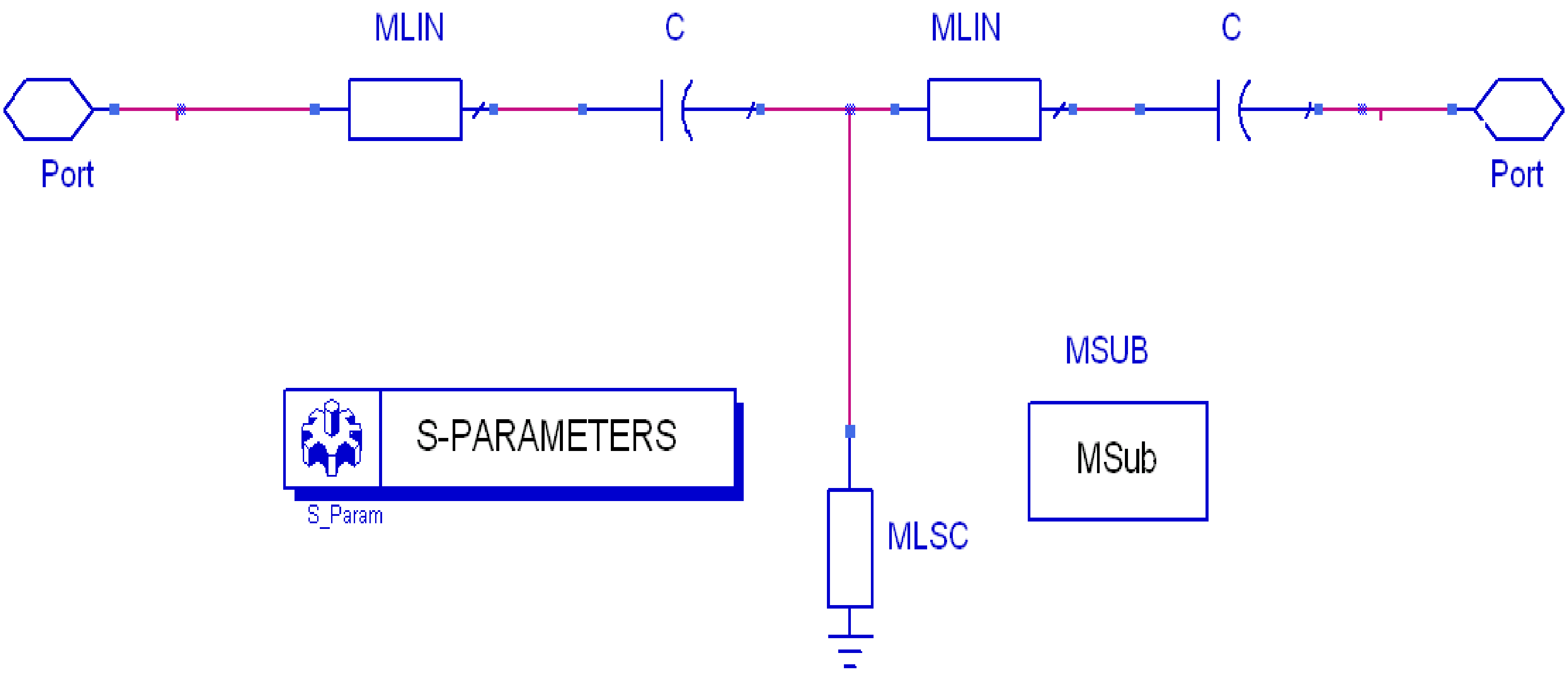


DOE Conclusion

- Output matching network is sensitive to the output match spec and is contributing significantly to the low yield

- Interstage matching network is also contributing to the low yield

Action: Redesign the Output Match



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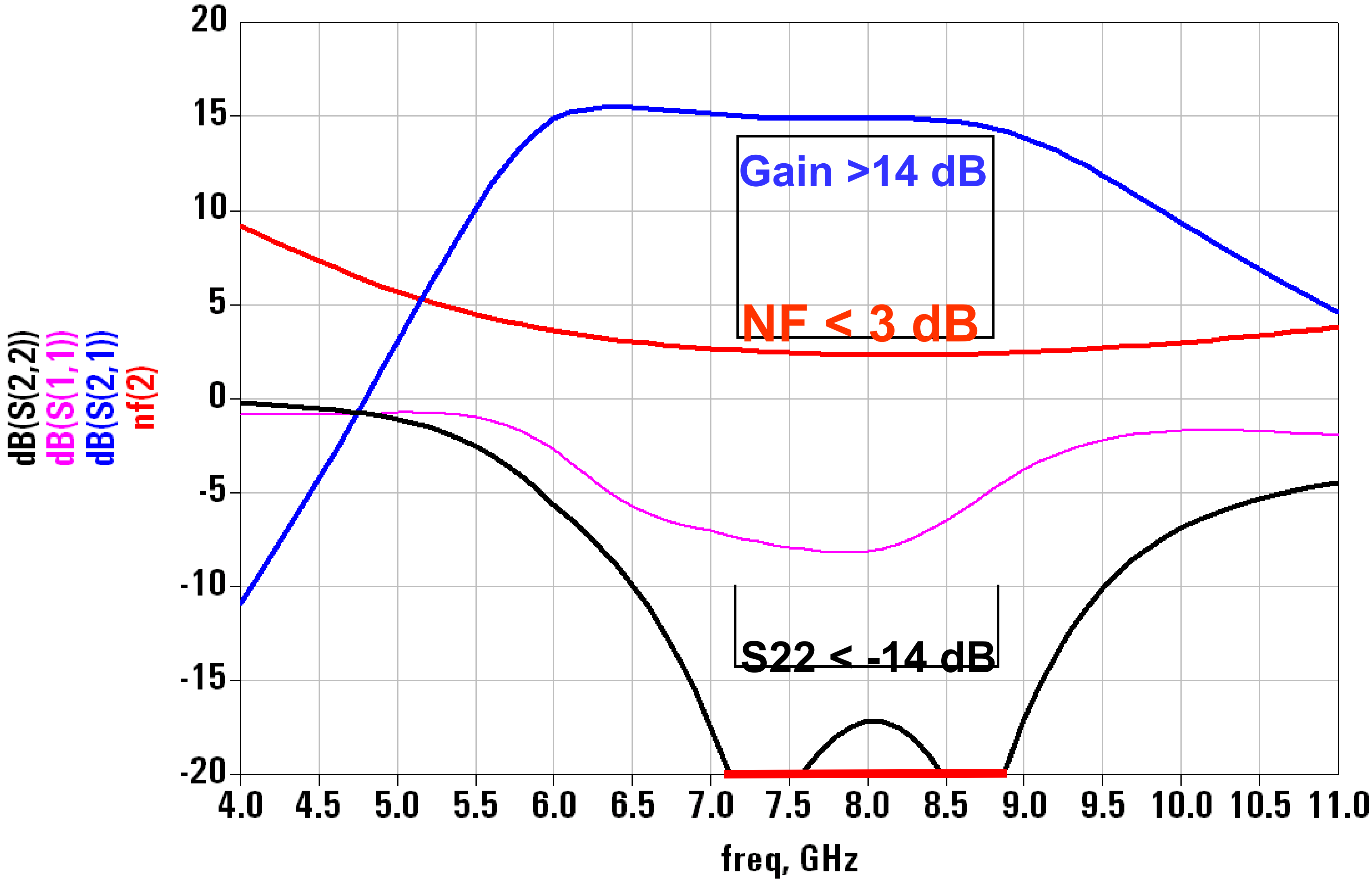
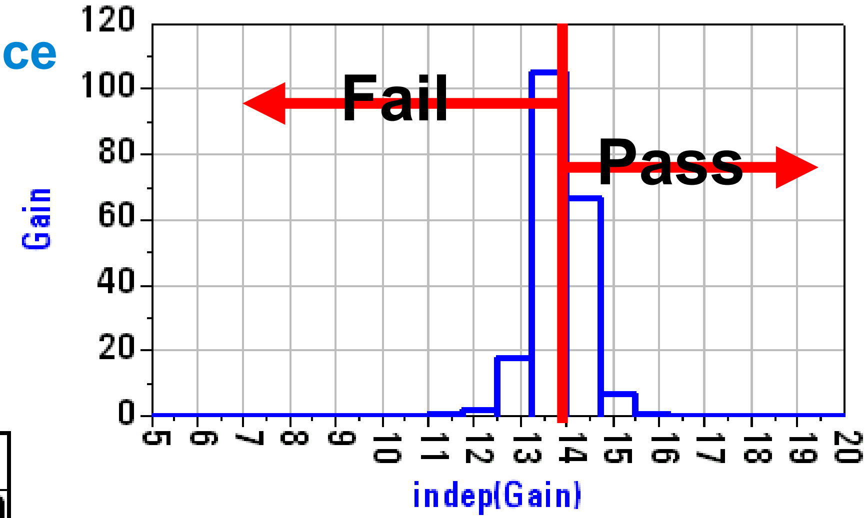
LNA Response with New Output Network



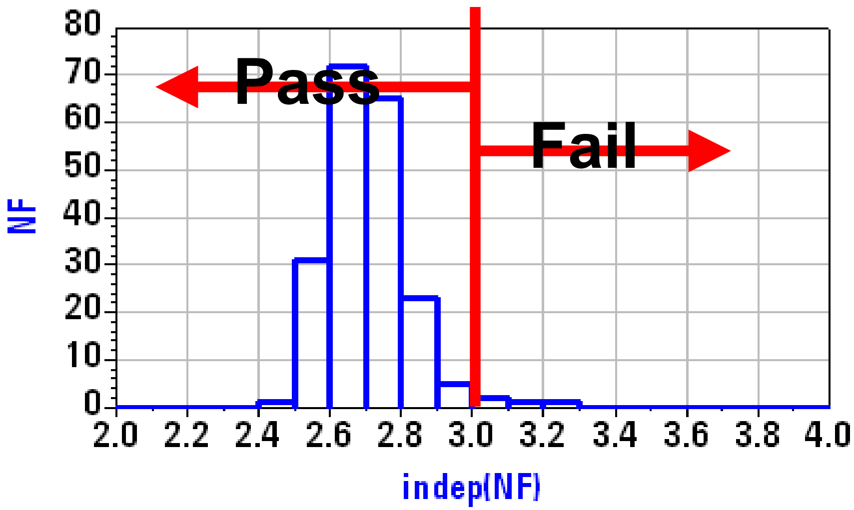
New Overall Yield of LNA : 39.5%

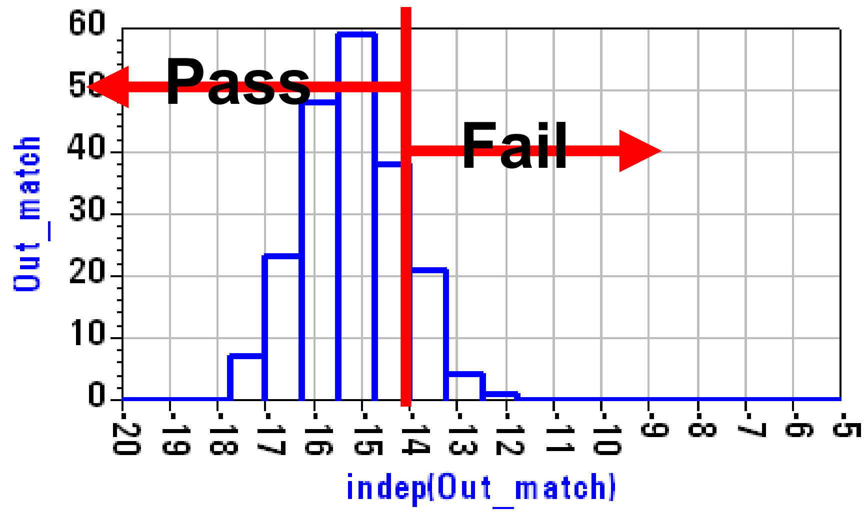


Statistical Analysis of LNA Performance

- 5% Gaussian variation in lumped
- Line widths vary ± 1/2 um
- Substrate height 100 um ± 3 um
- Substrate Er 12.9 ± 5%
- 42 FET samples

NumFail	NumPass	Yield
121.00	79.00	39.50





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MMIC Statistical Design Process

Obtain process parameters

Statistical device model or actual measured parameters

Start nominal design

Optimize design

Yield analysis

Sensitivity histograms / find sensitive network

Sensitivity analysis

DOE /find sensitive network

Design centering / yield optimization

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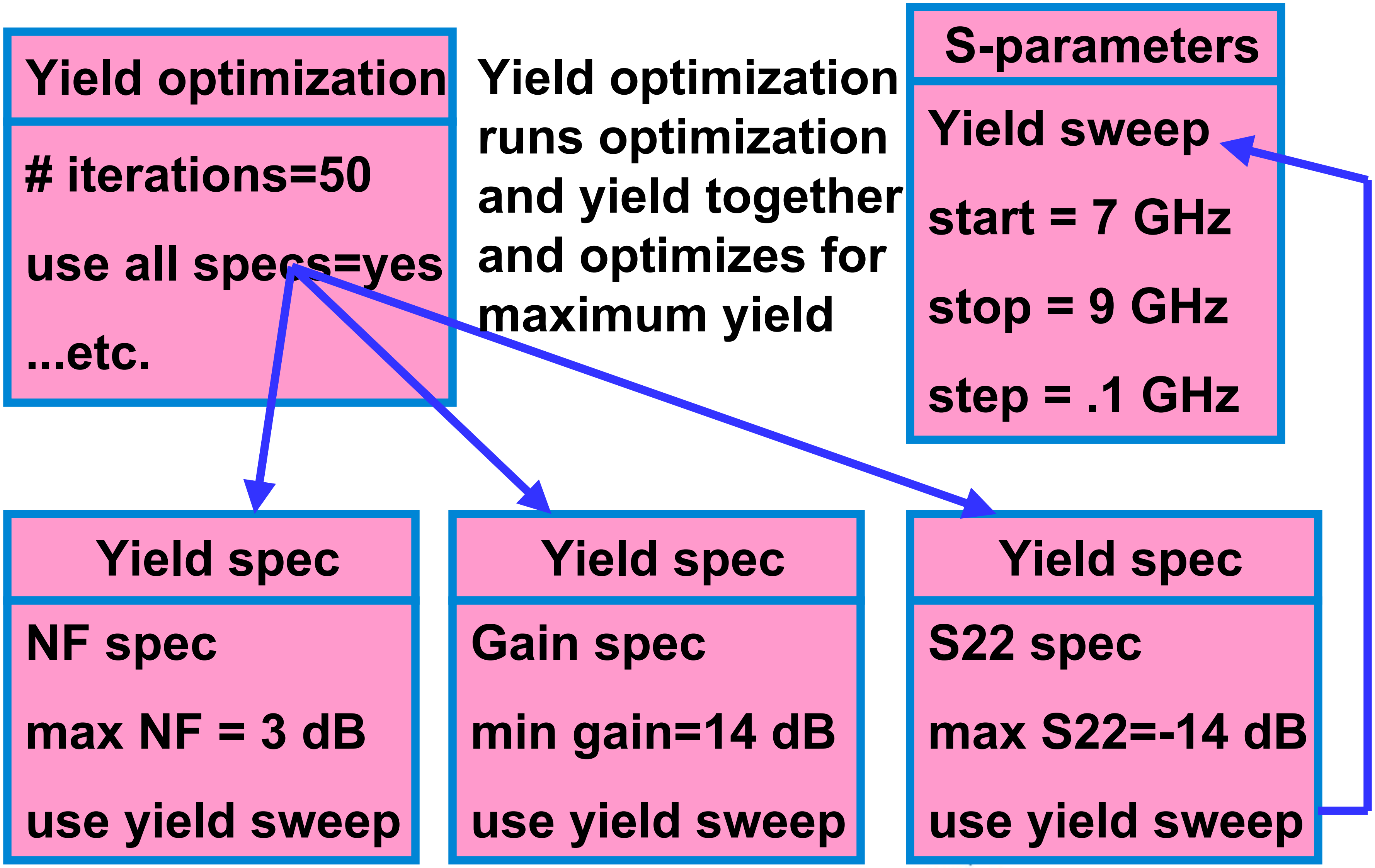
Yield Optimization (Design Centering)

<u>A Recap:</u>

- **We have reduced the sensitivity by redesigning the output matching network.**
- **The new matching network has also helped to reduce the output response variability span.**
- **Next we need to center the design for maximum yield using the yield optimization tool (also called design centering).**

"Design Centering" – Simplified Setup

Yield optimization runs optimization and yield together and optimizes for maximum yield



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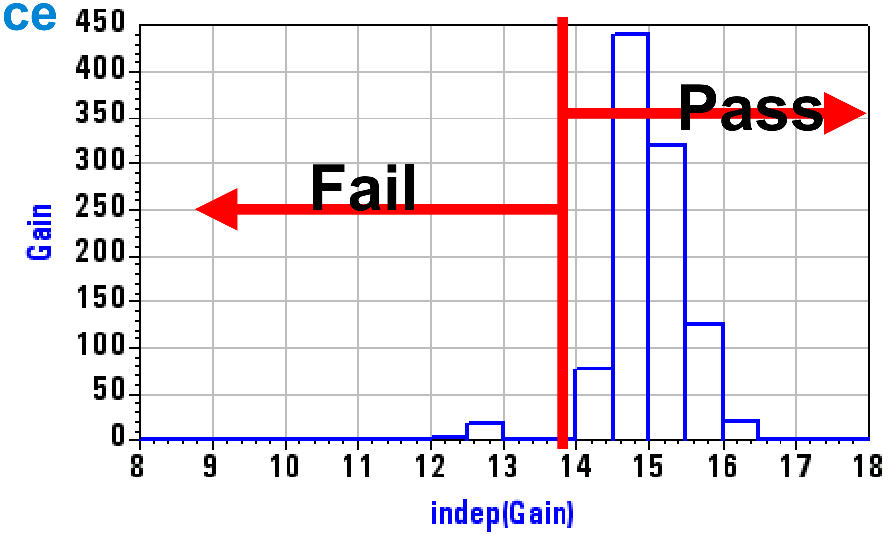
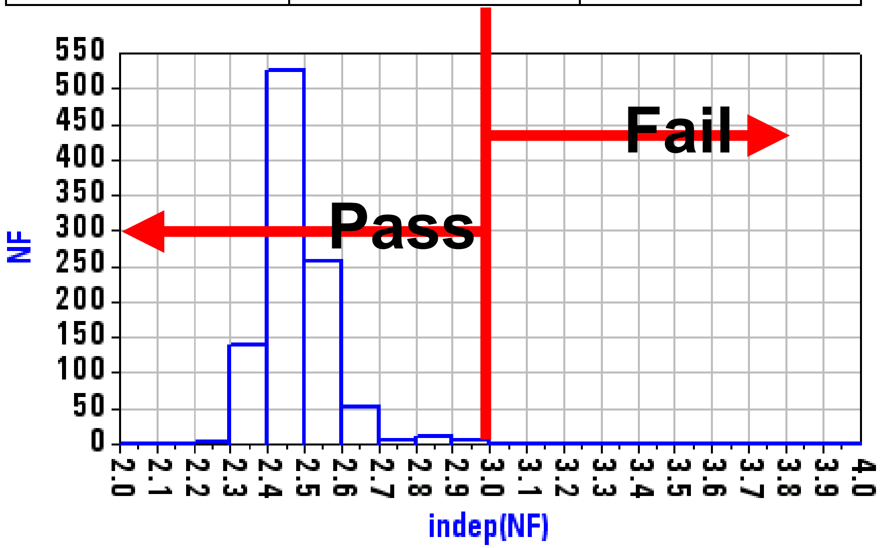
Final Yield after Design Centering: 97.4%

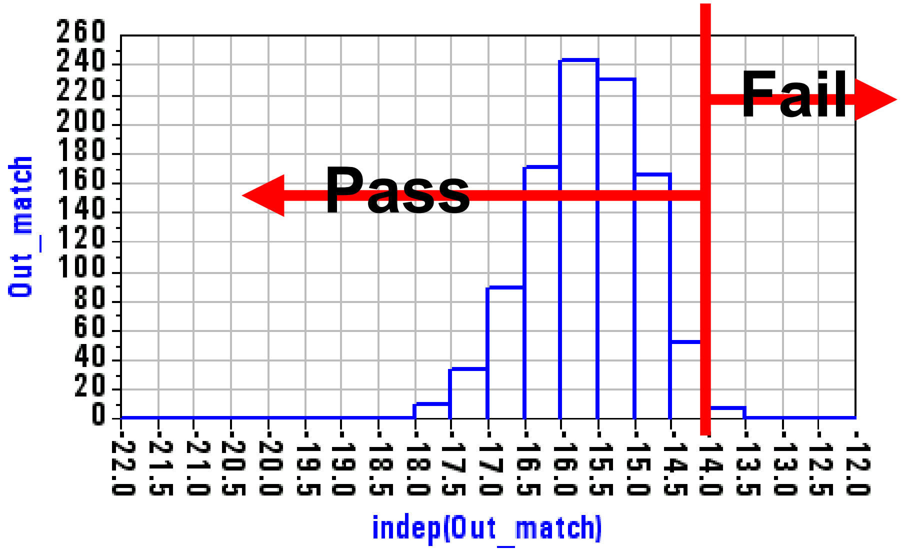
Statistical Analysis of LNA Performance

- 5% Gaussian variation in lumped
- Line widths vary ± 1/2 um
- Substrate height 100 um ± 3 um
- Substrate Er 12.9 ± 5%
- 42 FET samples

NumFail	NumPass	Yield
26.00	974.00	97.40







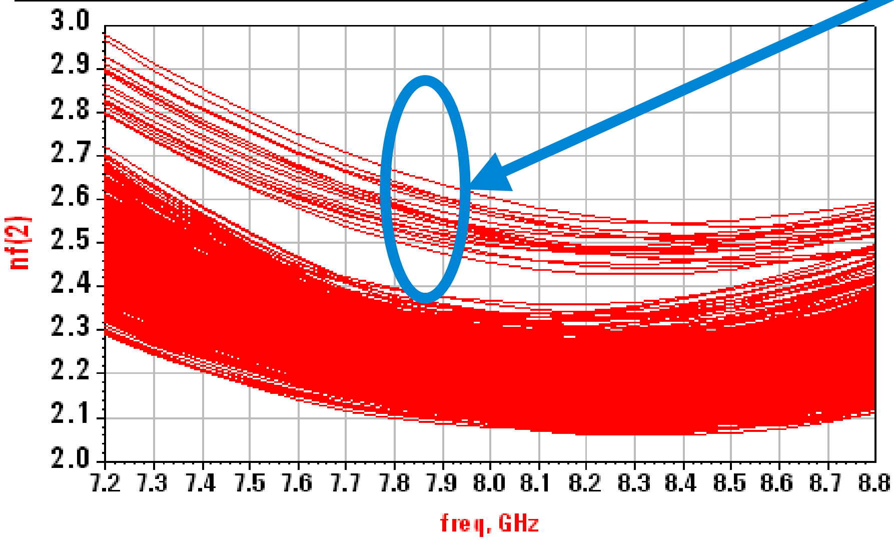
Response of Yield Trials

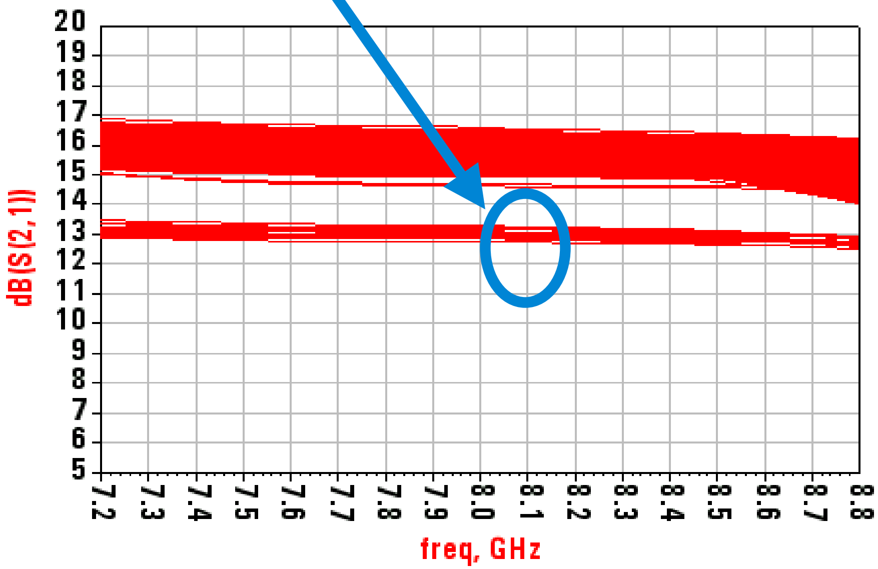
Statistical Analysis of LNA Performance

- 5% Gaussian variation in lumped
- Line widths vary ± 1/2 um
- Substrate height 100 um ± 3 um
- Substrate Er 12.9 ± 5%
- 42 FET samples

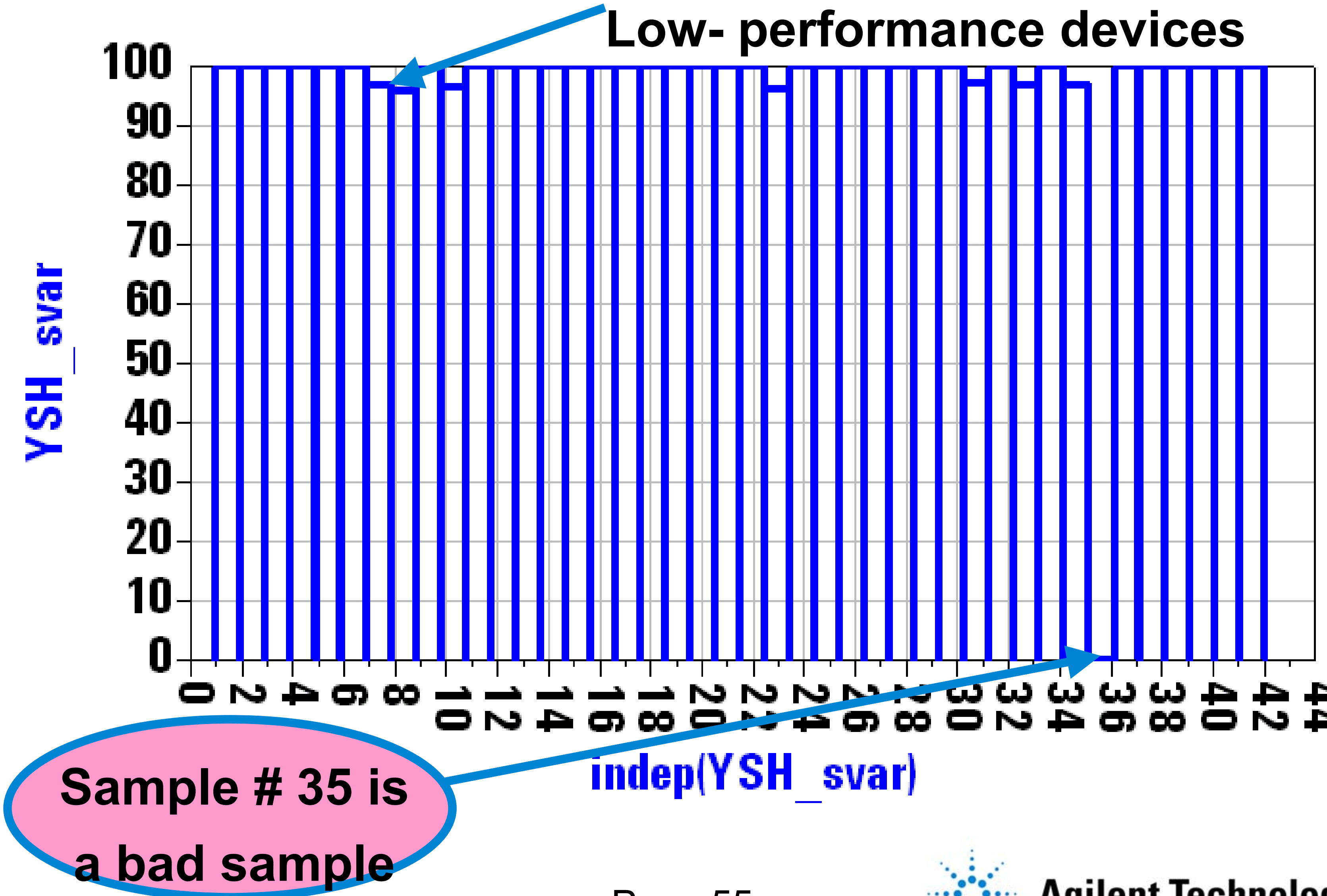
Note: Low- performance devices

NumFail	NumPass	Yield
26.00	974.00	97.40

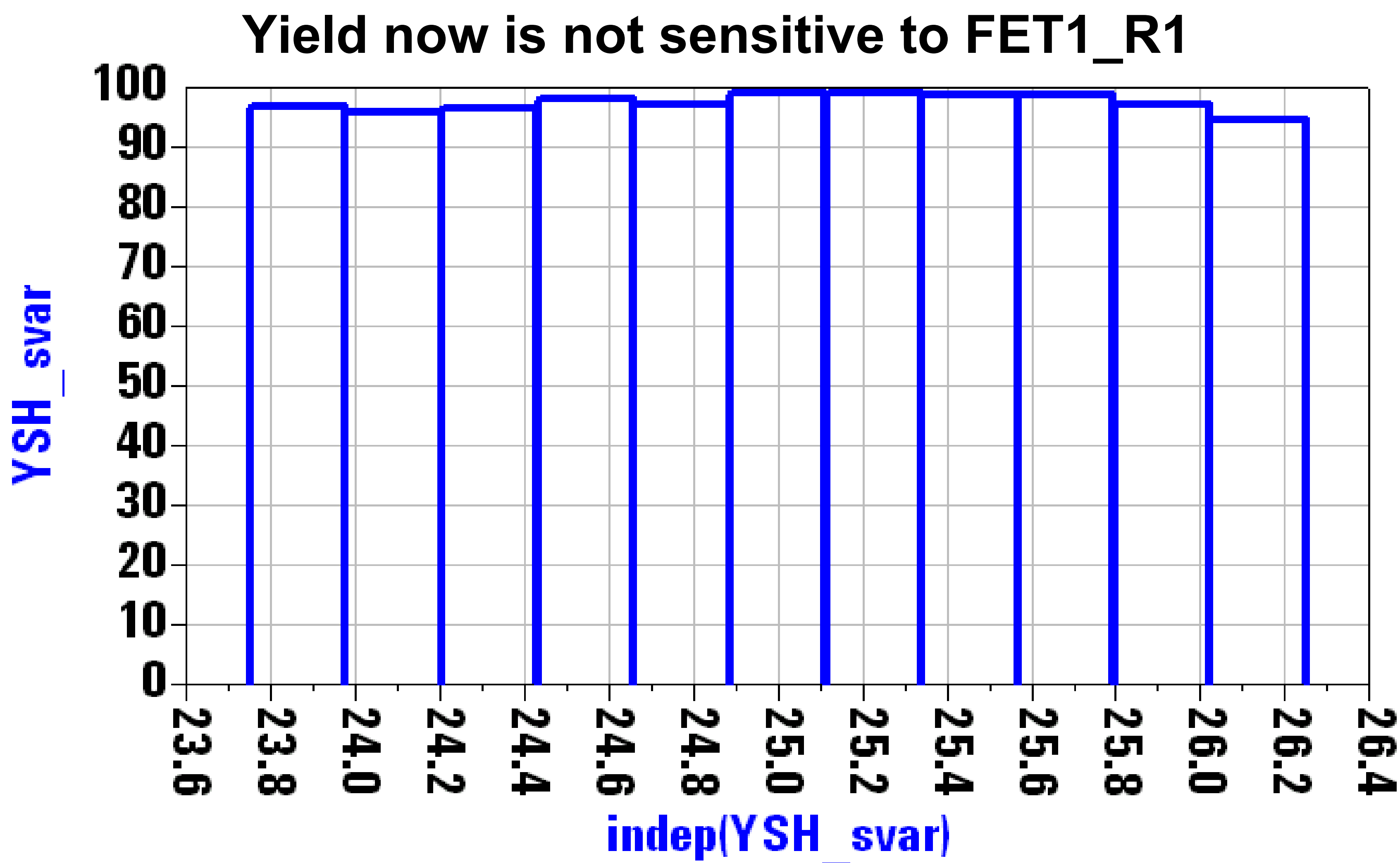




Yield Sensitivity with Respect to Sample



Yield Sensitivity with Respect to FET1_R1



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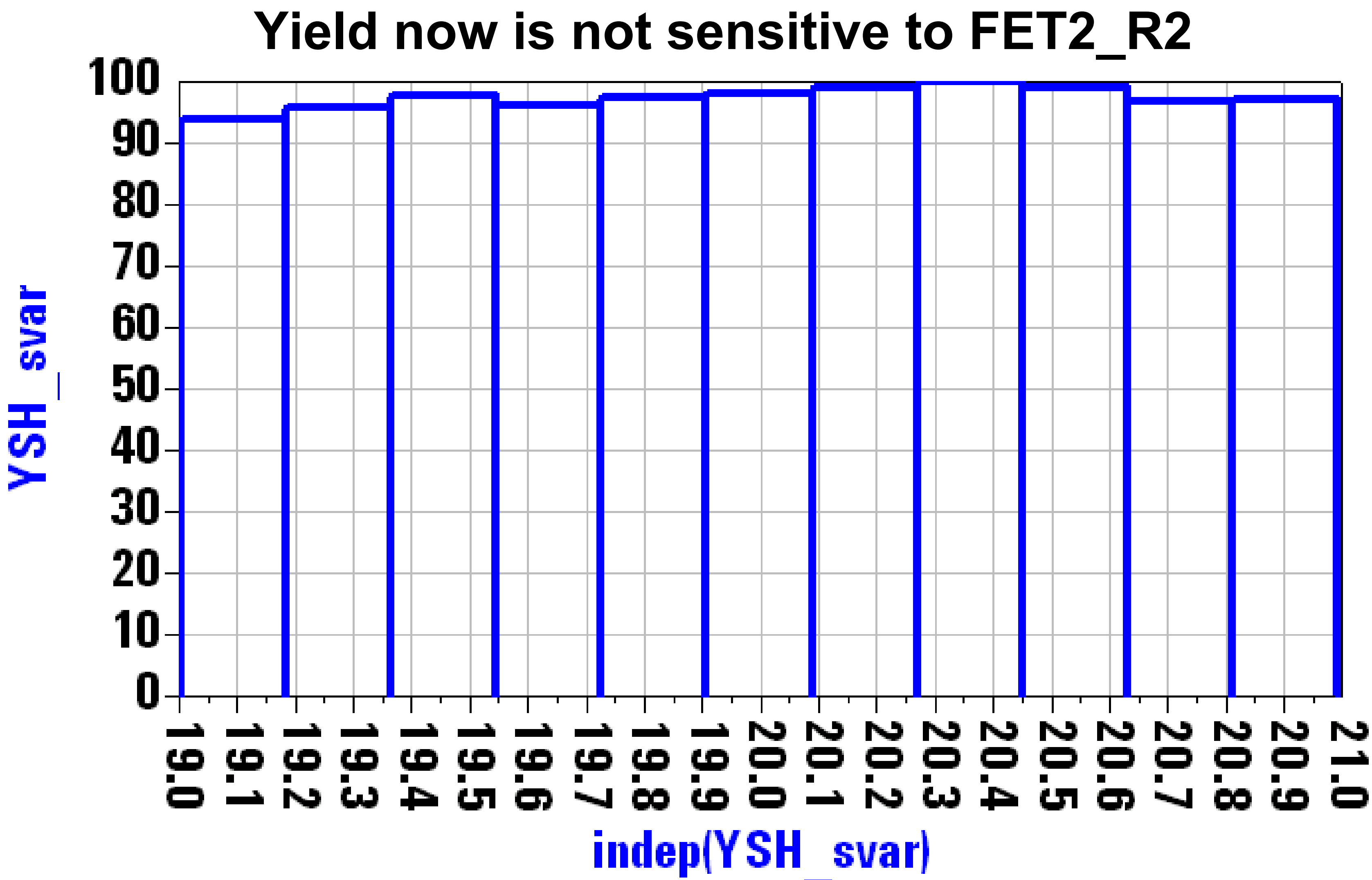
Yield Sensitivity with Respect to FET2_R2



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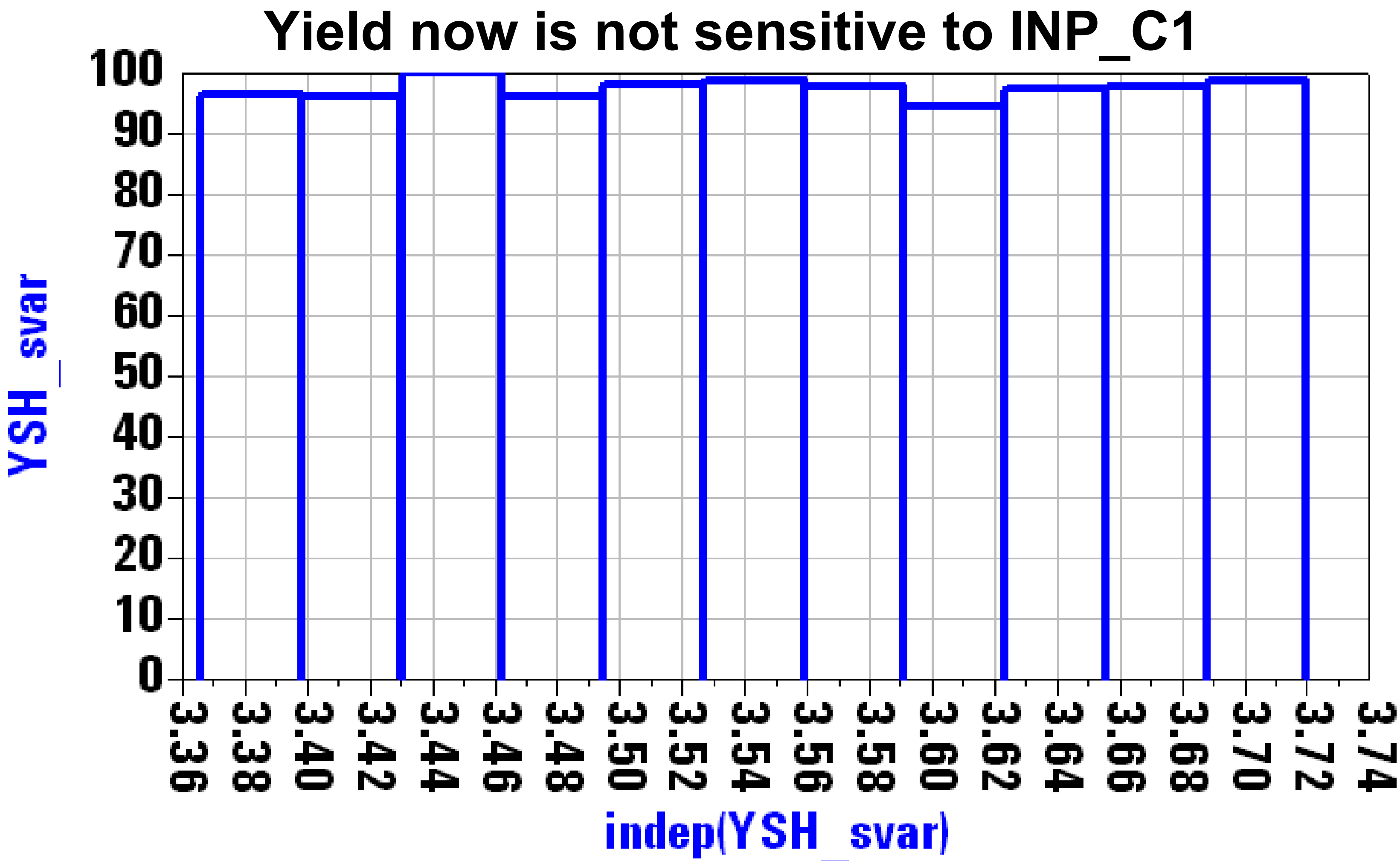
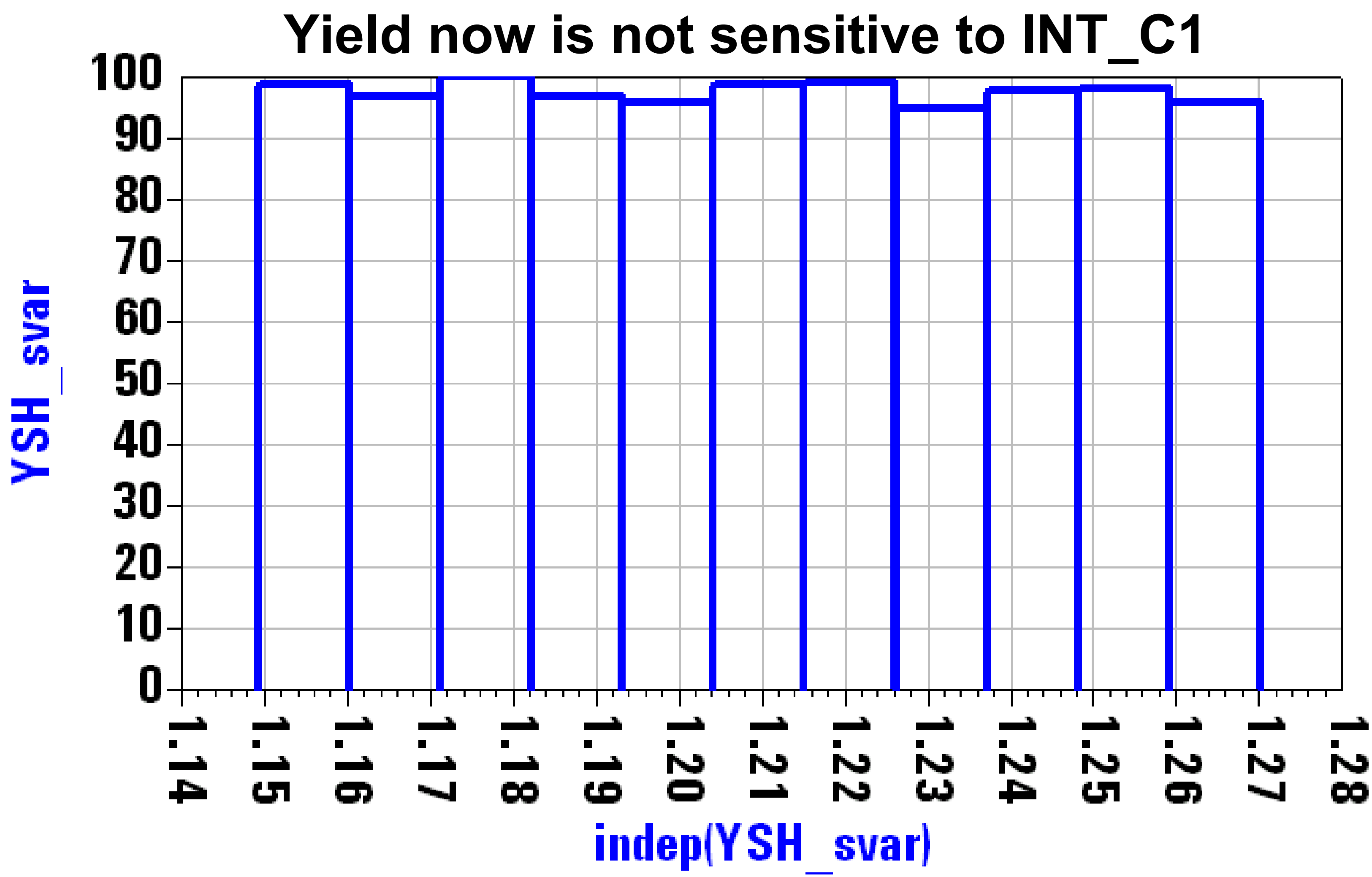
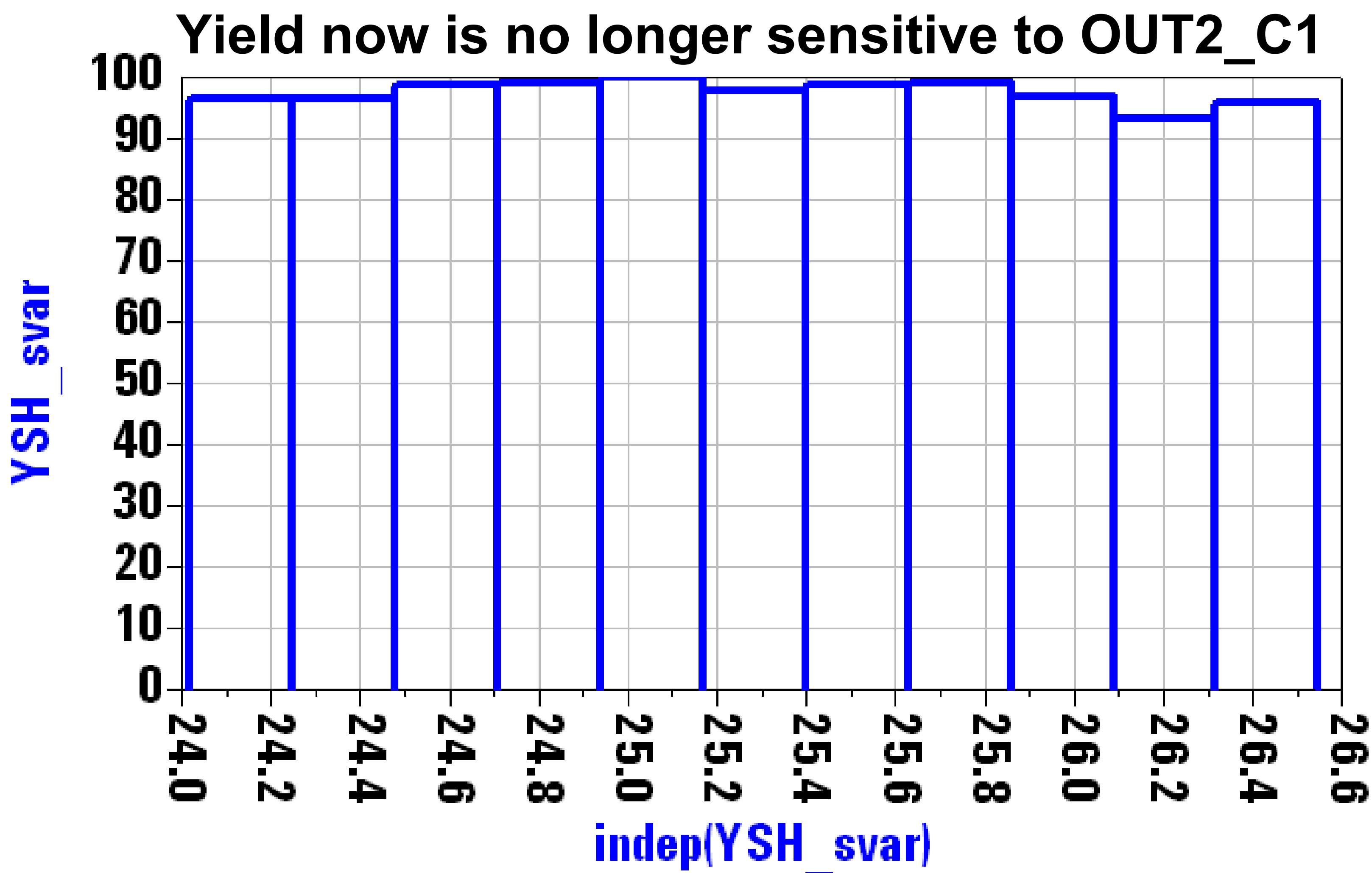
Yield Sensitivity with Respect to INP_C1



Yield Sensitivity with Respect to INT_C1



Yield Sensitivity with Respect to OUT2_C1



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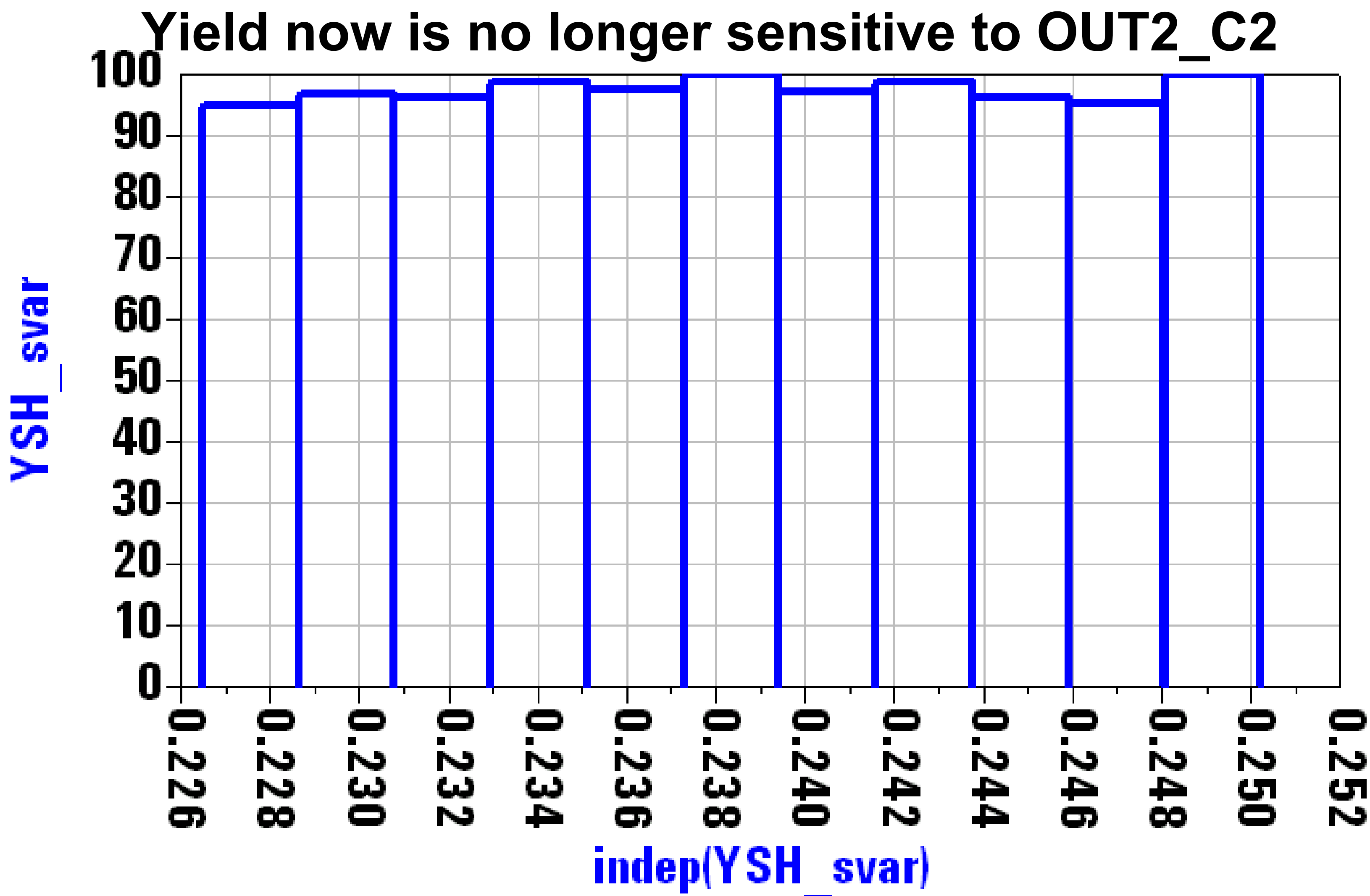
Yield Sensitivity with Respect to OUT2_C2



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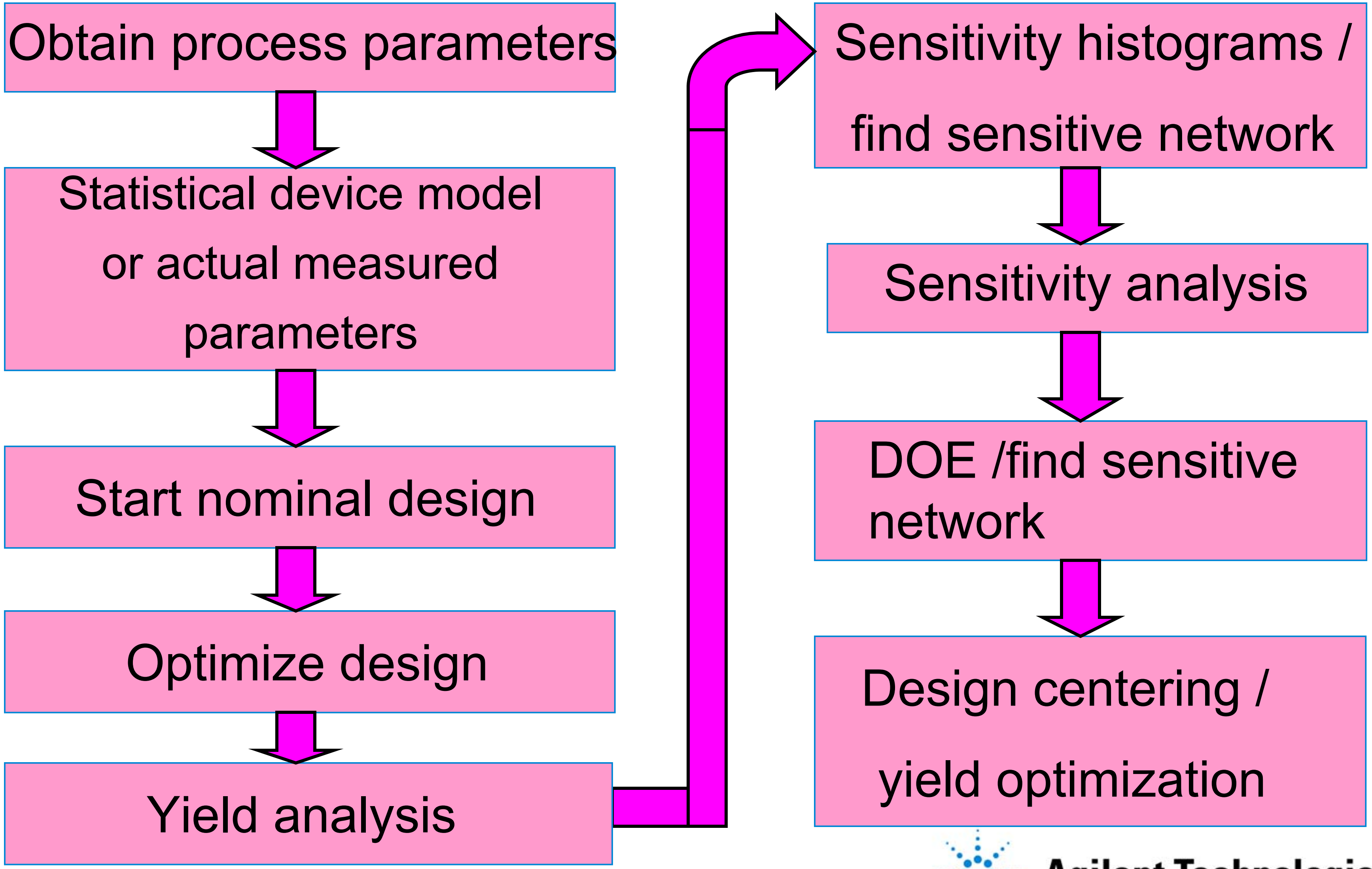
Recap: MMIC Statistical Design Process



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Conclusion (ADS 2001 Statistical Design Package)

- Advanced optimization technique
- Yield analysis
- Yield optimization or design centering
- Sensitivity analysis
- Design of experiment (DOE) with full supporting plots.
- Yield sensitivity histograms.
- Correlation analysis with any kind of distribution, including log normal distribution, which is heavily used in RFIC design.
- Mismatch models statistical analysis of devices from different sites on the wafer, from different wafers, and from different lots.

Appendix A

A Brief Tutorial on

Design of Experiments (DOE)

DOE – A Brief Tutorial

Start by choosing variables that affect the response

Choose three variables with their +1 and -1 :

Width of lines (W)	**W=W_nom ± .5 um**
Resistors (R)	**R= R_nom ± 5%**
Capacitors (C)	**C= C_nom ± 5%**

Example: For W

-1 corresponds to 9.5 um

+1 corresponds to 10.5 um

0 corresponds to nominal value, 10um

Main Effect of Capacitors, C on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

Average gain for C=-1

13.7725 dB (yellow)

Average gain for C=1

13.86 dB (blue)

Slope= .044

Main Effect of Resistors, R on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

Average gain for R=-1

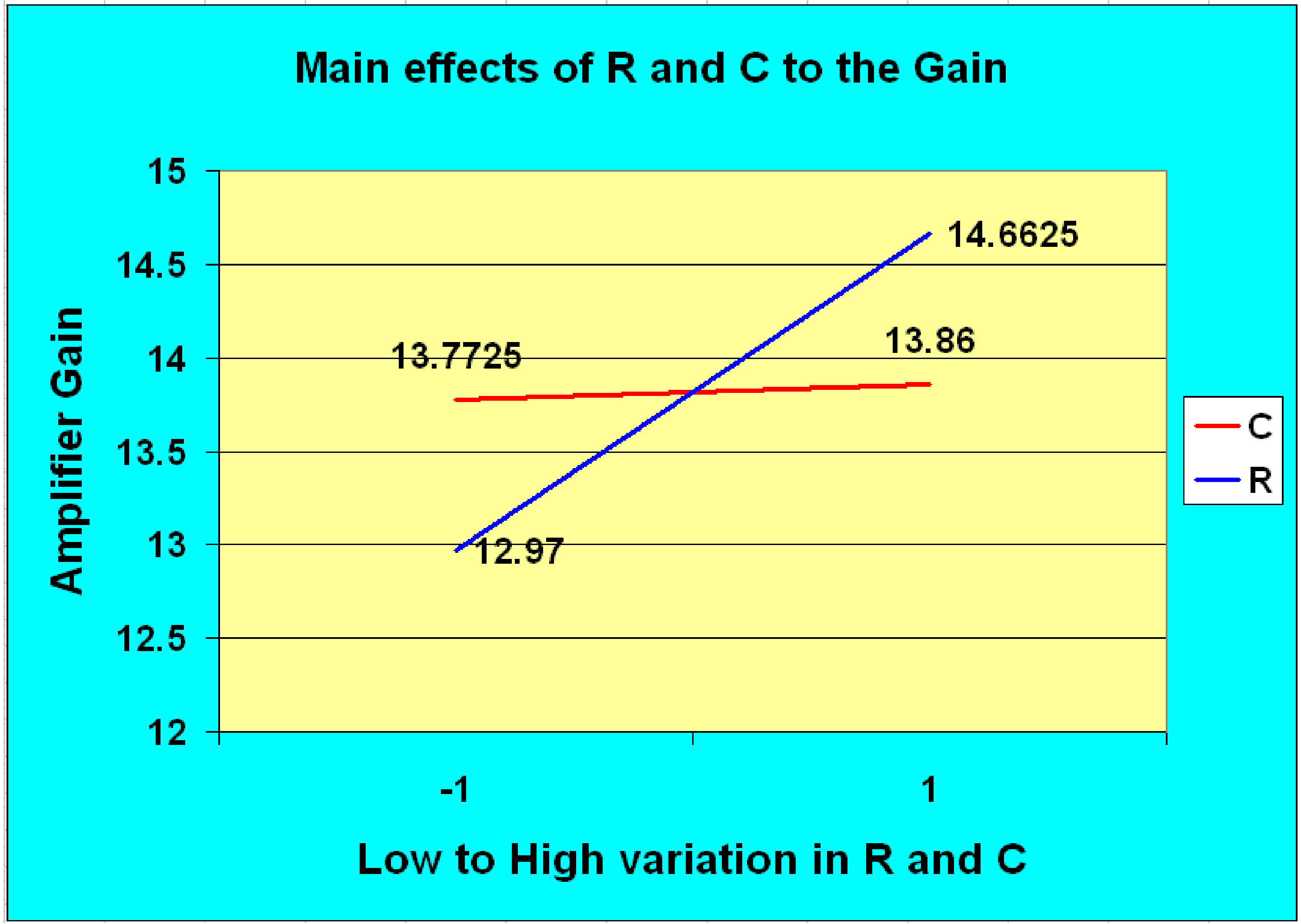
12.97 dB (blue)

Average gain for R=1

14.6625 dB (green)

Slope = .85

Plotting Main Effects of C and R



Interaction Effect of (W and R) on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

Average gain for W*R=-1

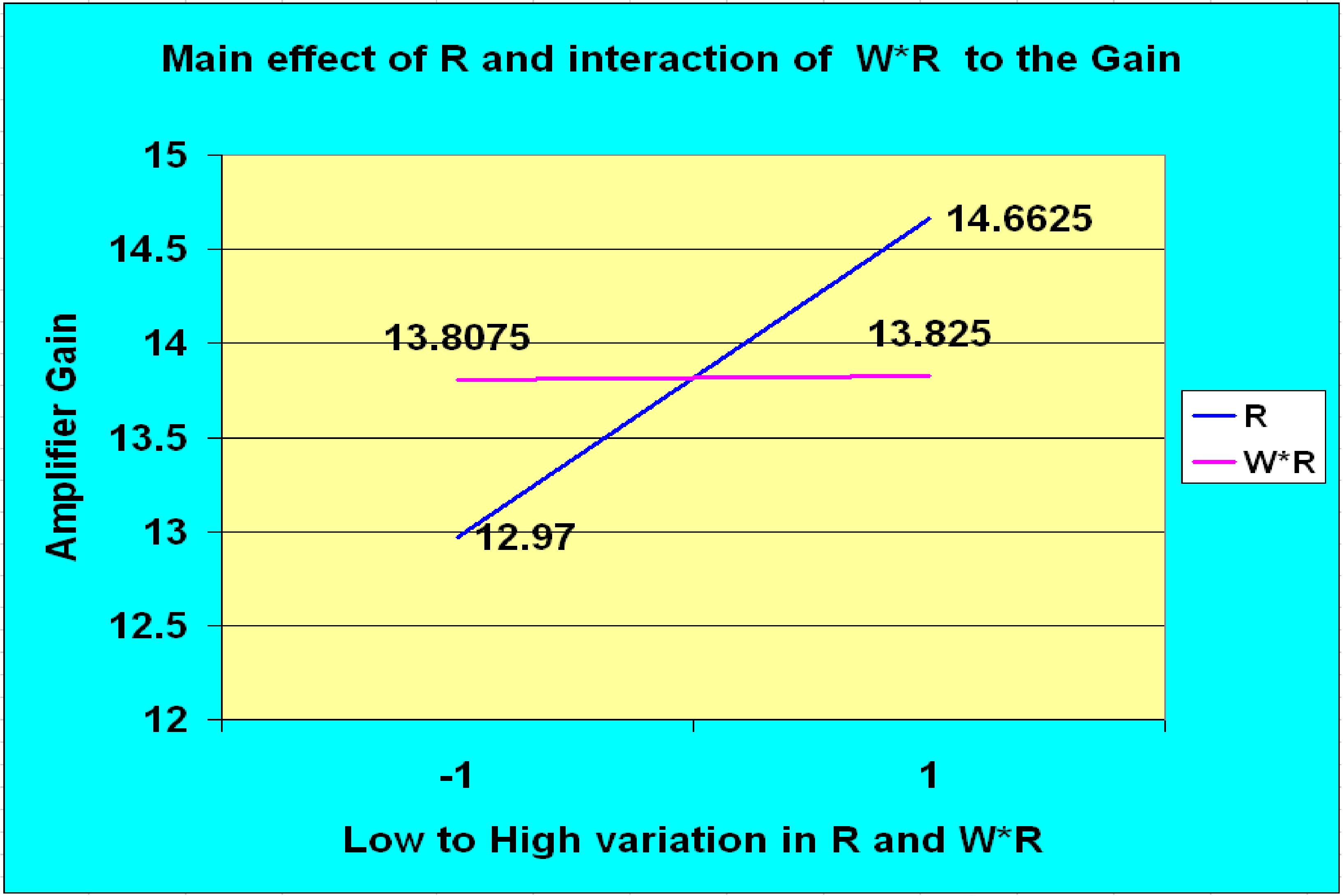
13.8075 dB (blue)

Average gain for W*R=1

13.825 dB (pink)

Slope = .0088

Plotting Interaction Effects of W and R



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Obtaining the Rest of the Coefficients

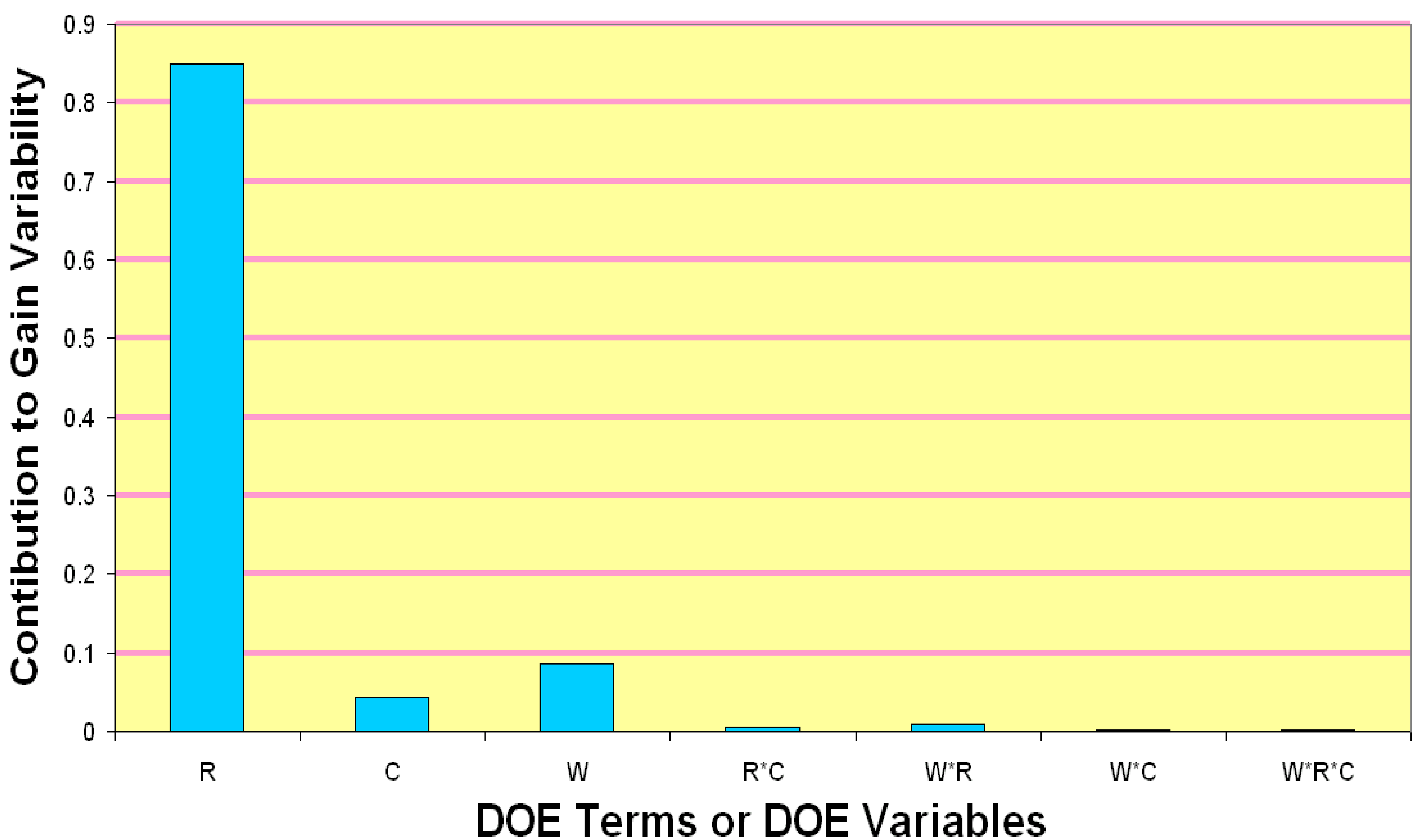
Term	Coefficient
Constant (nominal gain)	13.8
W	.09
R	.85
C	.044
W*R	.0088
W*C	.0013
R*C	.0050
W*R*C	0.0025

We calculated these three coefficients in the previous slides

Construct a linear equation to represent the experiment results.

Gain=13.8+.09W+.85R+.044C+.0088WR+…..etc.

Display All Effects on a Pareto Chart



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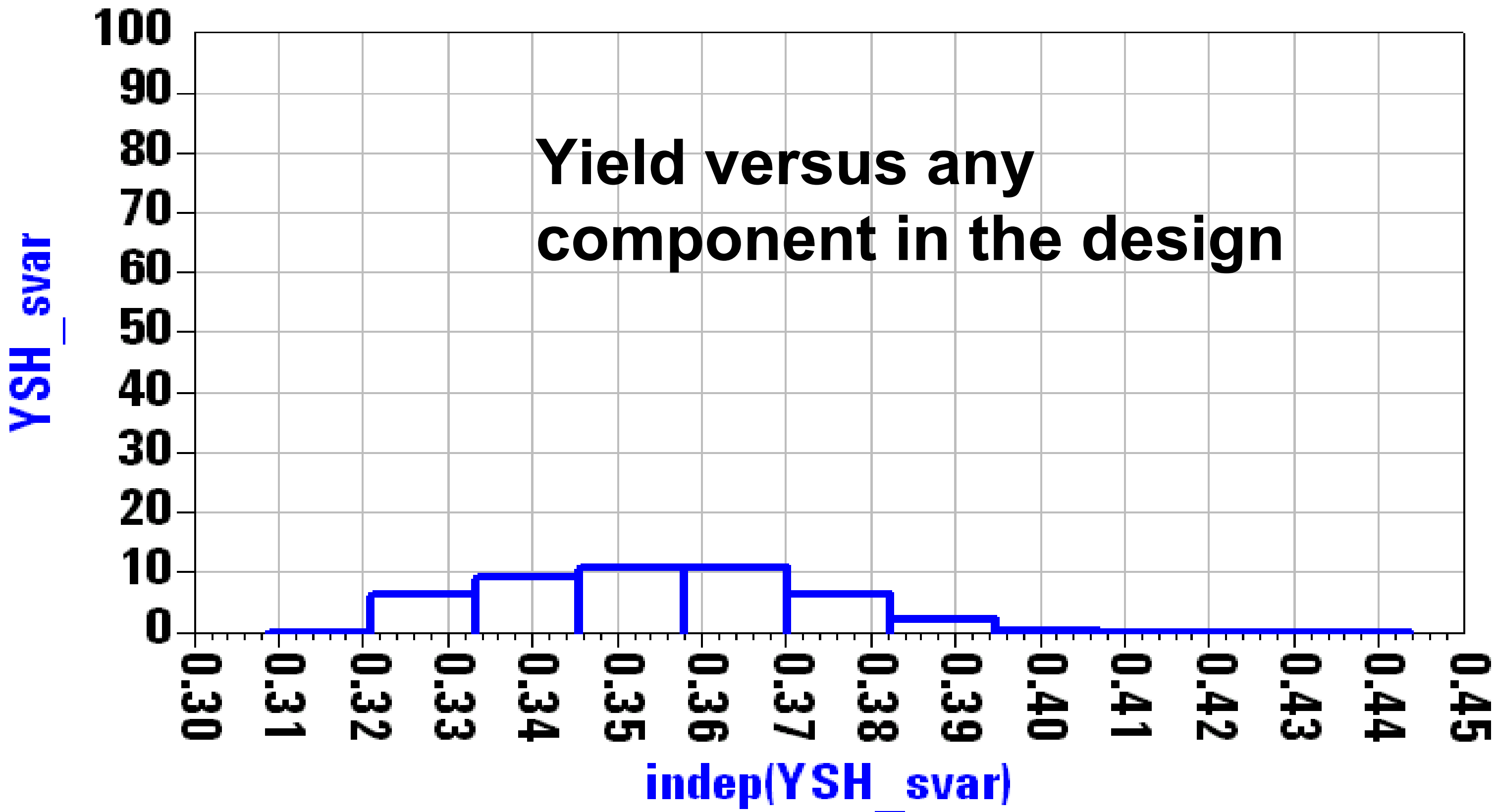
Appendix B

Yield Sensitivity Histograms Used in Trade-off Study

Start with This Scenario

- System people are badly in need of an X-band LNA immediately
- An old design is available, but it might not meet the required specs
- Run yield analysis on the existing design
- Use the yield sensitivity histograms to make wise decisions about how to use this design.

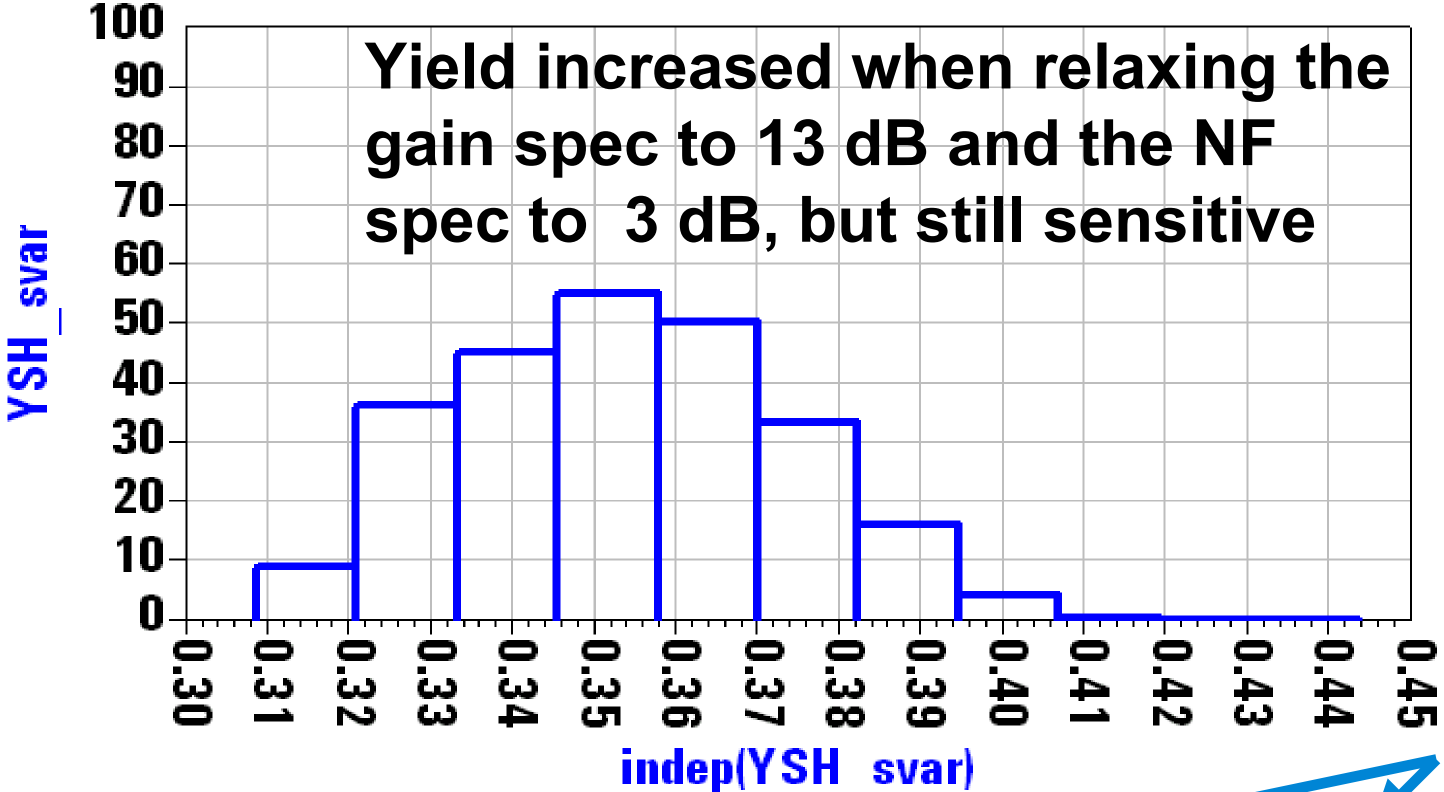
Existing Amp Has Low Yield to the Specs



Eqn NF_Spec_Min=0	Eqn NF_Spec_Max = 2.8
Eqn Gain_Spec_Min = 14.0	Eqn Gain_Spec_Max=100
Eqn S22_Spec_Min=-100	Eqn S22_Spec_Max=-14

Initial specs

Relax the NF Spec to 3 dB and Gain to 13 dB



Eqn NF_Spec_Min=0

Eqn Gain_Spec_Min = 13.0

Eqn S22_Spec_Min=-100

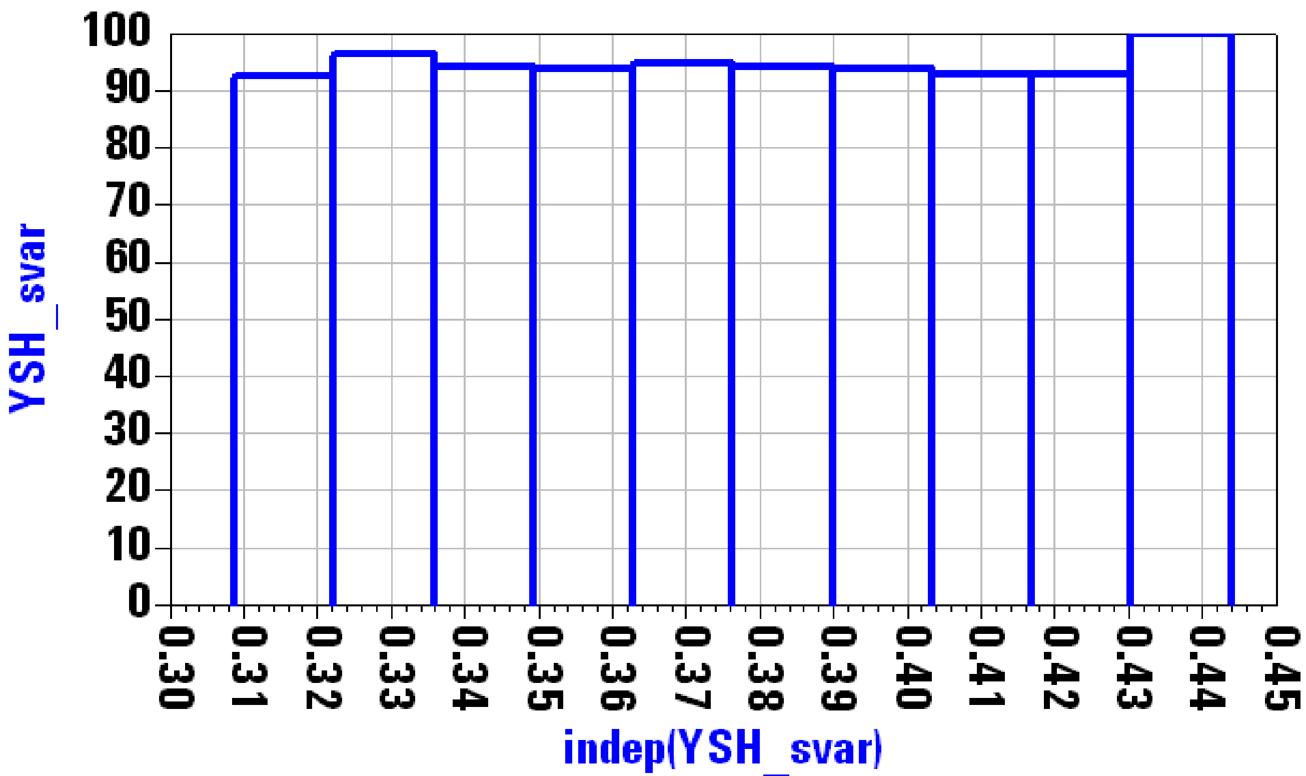
Eqn NF_Spec_Max = 3.0

Eqn Gain_Spec_Max=100

Eqn S22_Spec_Max=-14

Change specs slightly and watch the corresponding yield immediately

Drop S22 Spec and Use Amp as Balanced



Eqn NF_Spec_Min=0

Eqn NF_Spec_Max = 3.0

Eqn Gain_Spec_Min = 13.0

Eqn Gain_Spec_Max=100

If we drop the S22 spec, yield goes up to >90.

This means that we can successfully use the LNA if we use it in a balanced configuration with Lange couplers.